DesignCon 2015

SerDes Steady State Adaptation Challenges in Existing SAS/SATA and Emerging PCIe Gen4/SAS4 Application and their Solutions with Pattern Discriminator Constrained Adaptation

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Agenda

- Time Varying Transceiver System
- Channel Revisit
- Channel Loss Variability Demonstration with Simulation
- Silicon Characteristics Changes with Temperature
- Time and Frequency Domain View of Pattern Characteristics
- Spectral Contents of Some Commonly Used Patterns
- Pattern Discriminator Assisted Adaptation
- Tone Discriminator Equivalence to FFT
- An Example Pattern Discriminator Operation on CJTPAT
- Pattern Discriminator Architecture
- Pattern Discriminator Assisted Adaptation
- SAS/SATA/FC 8b/10b Pattern Evaluation
- PCIe Gen3/Gen4 and SAS4 Evaluation with PD
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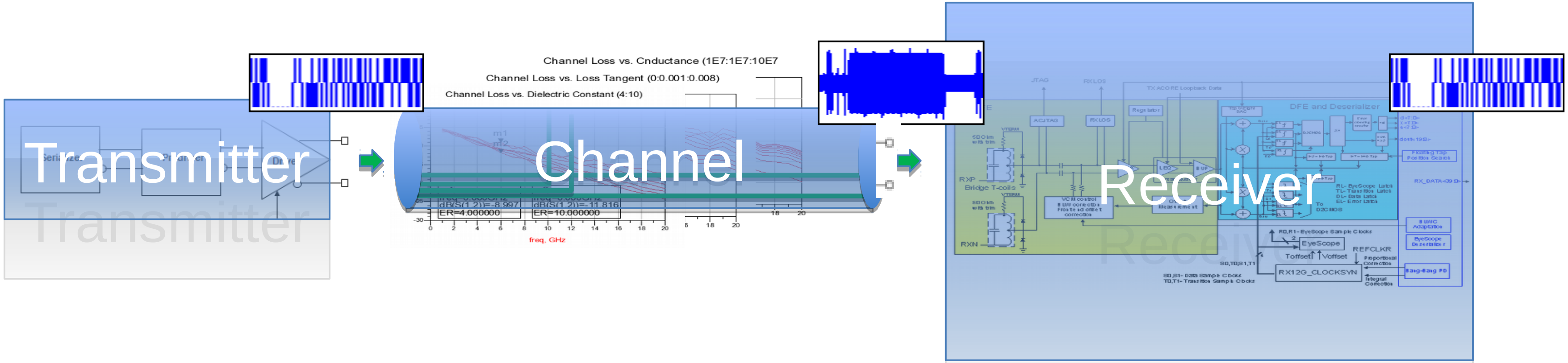
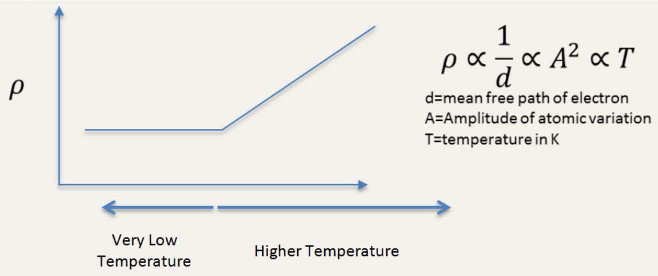
Time Varying Transceiver System

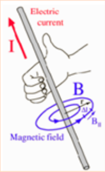
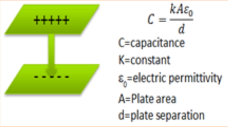
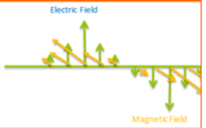


- Transmitter/Receiver silicon characteristics changes with temperature and voltage variation over time
- Channel loss behavior changes over time due to temperature dependent variations of
  - Dielectric constant
  - Conductance
  - Loss tangent
- A transceiver is required to re-adapt for coping with channel and silicon characteristics changes
- Many existing standard does not guarantee spectrally rich patterns to support re-adaptation

Channel Revisit

- Low frequency electrical resistance $R = \rho\frac{L}{A}$ with ρ=resistivity, L=Length of conductor, A=area of conductor cross section; ρ in a conductor arises due to collision process inside the wire
  - Collision increases with increased temperature
- Electro-magnetic view of high frequency electrical medium loss
  - Magnetic fields, B, are produced due to current flow
  - Electric fields, E, are produced between opposite charge carrying plates
  - Electric and magnetic fields are orthogonal to each other



Magnetic Field	Electric Field	Orthogonal Electric and Magnetic Field
 **Source:** **http://hyperphysics.phy-astr.gsu.edu/hbase/magnetic/magcur.html#c3** **Magnetic field due to current flow**	 Electric field and Capacitance from parallel plates	 Orthogonal relationship between electric and magnetic fields

- http://hyperphysics.phy-astr.gsu.edu/hbase/electric/restmp.html#c1
- http://hyperphysics.phy-astr.gsu.edu/hbase/magnetic/magcur.html#c3
- http://hyperphysics.phy-astr.gsu.edu/hbase/electric/elefie.html#c1

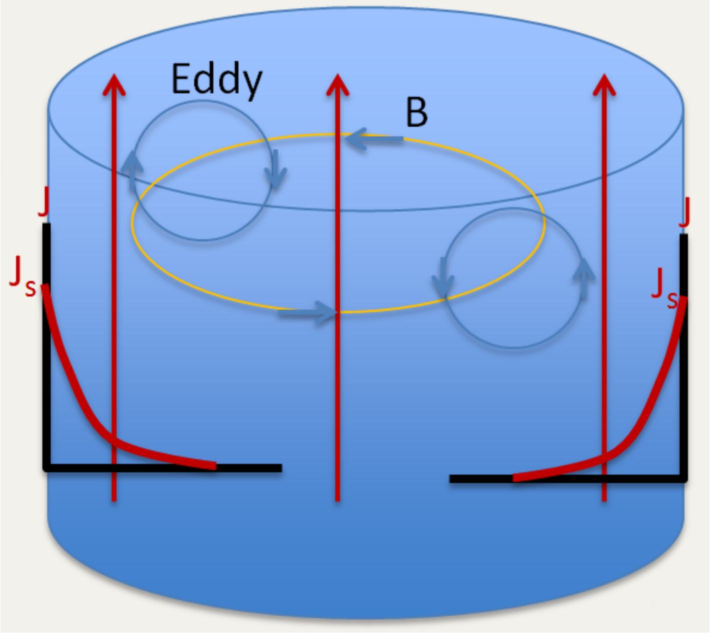
Channel Revisit

- Current through a conductor creates magnetic field which in turn creates Eddy current
- Inside conductor Eddy current opposes the current and near outside surface Eddy current reinforces the current resulting in skin effect
- Due to skin effect at high frequency most current is closer to the outside surface and current density drops inside the conductor as a function of

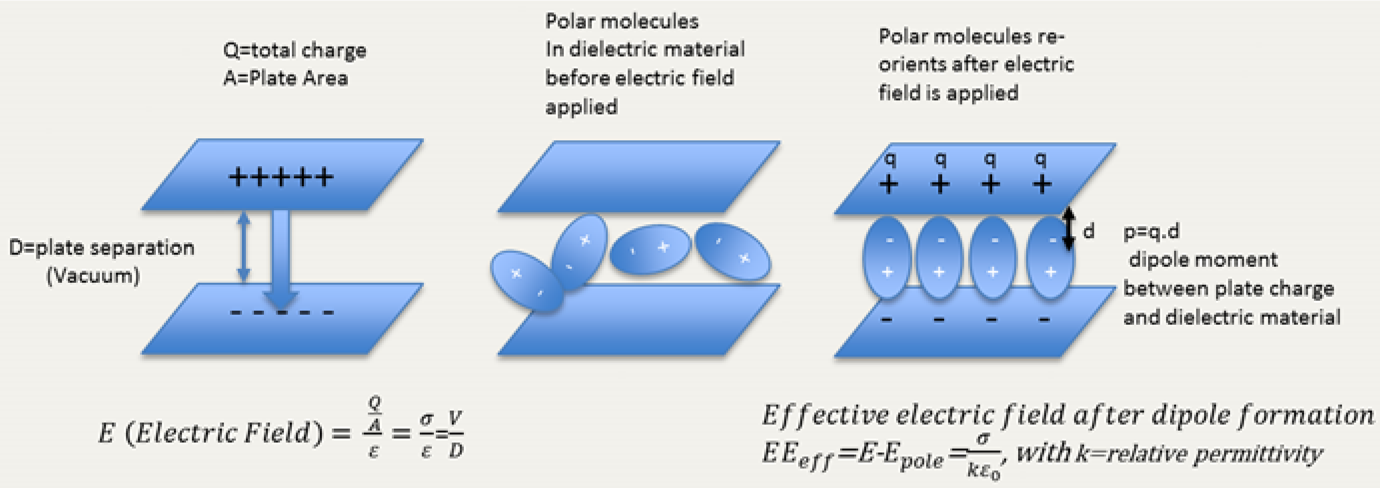
$$J(T,f) = J_s e^{(-\frac{d}{\delta})}, with\ \delta = \sqrt{\frac{2\rho}{w\mu_r\mu_0}} \propto \frac{T}{\sqrt{f}}$$

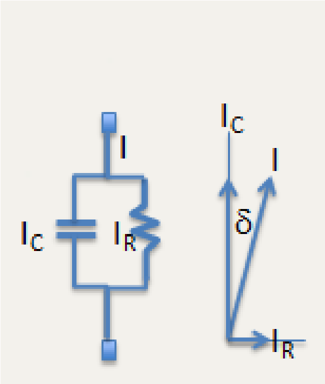
Where,
J_s = current density,
d = depth from surface,
δ = skin depth where current is $\frac{1}{e}$ of the surface,
ρ = resistivity of the conductor,
$\omega = 2\pi f$ is the angular frequency of the signal,
μ_r = relative magnetic permeability of the conductor,
μ = permeability at vacuum.
If conductor thickness is larger than skin depth, the AC resistance increases by $\sqrt{f}$

- At high frequency when most of the current flows through the surface, surface roughness increases effective electrical path
- http://hyperphysics.phy-astr.gsu.edu/hbase/electric/skineffect.html
- http://en.wikipedia.org/wiki/Skin_effect Stephen H. Hall, et al, "Advanced signal integrity for high speed digital designs", Wiley, IEEE



Channel Revisit





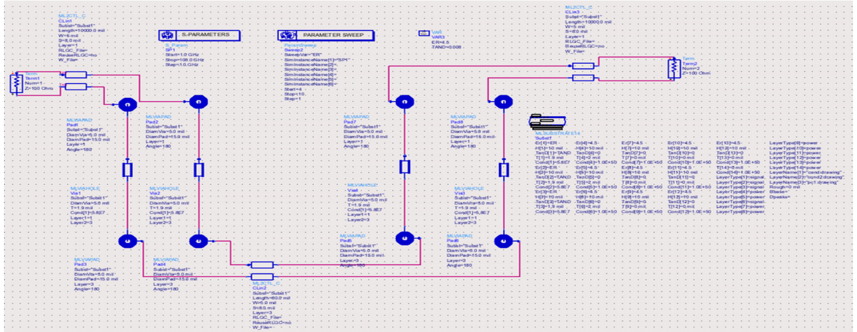
Loss tangent model

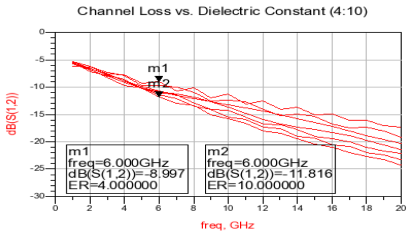
- Polar molecules with random orientation fills the gap between traces in a PCB
- Part of the applied electric field is used to orient the polar materials
- At high frequency signaling significant energy is dissipated to orient and reorient the polar materials.
- The electric model of this imperfection consists of a capacitor with ideal dielectric in parallel with a resistor

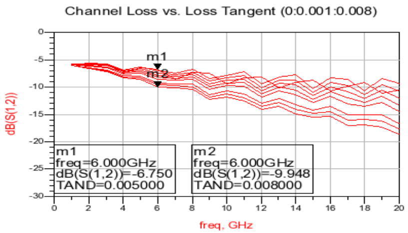
http://hyperphysics.phy-astr.gsu.edu/hbase/electric/dielec.html
Scott Hinaga, Technical Leader, PCB Technology Group, Cisco Systems, Inc., et al
“Thermal Effects on PCB Laminate Material Dielectric Constant and Dissipation Factor”
Jason R. Miller et al., “Temperature and moisture dependence of PCB and package traces and the impact on signal performance”, DesignCon 2012

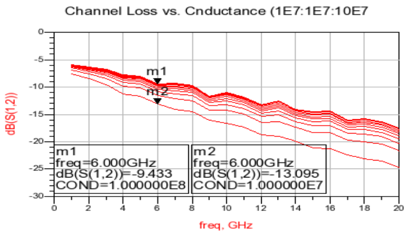
Channel Loss Variability Demonstration with Simulation

- A good measured channel parameter variability is presented in "Jason R. Miller et al., "Temperature and moisture dependence of PCB and package traces and the impact on signal performance", DesignCon 2012"
- Temperature dependence of channel characteristics changes is demonstrated using simulated channel as a function of
  - Conductance change
  - Dielectric change
  - Loss tangent change



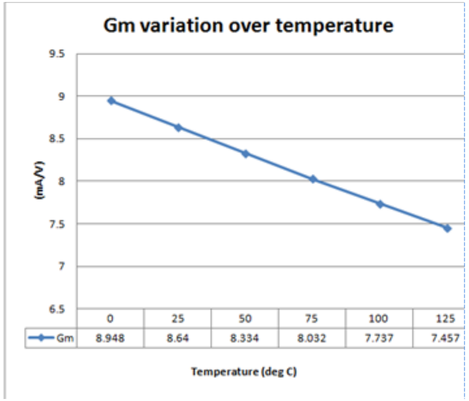


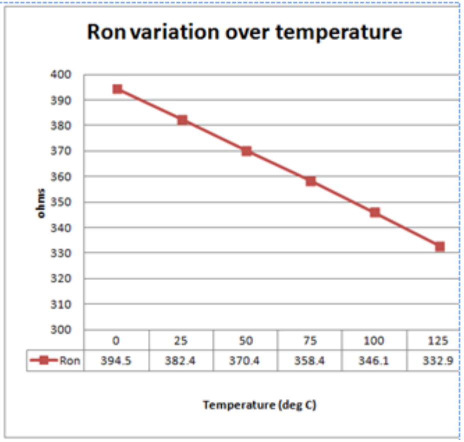




Silicon Characteristics Changes with Temperature

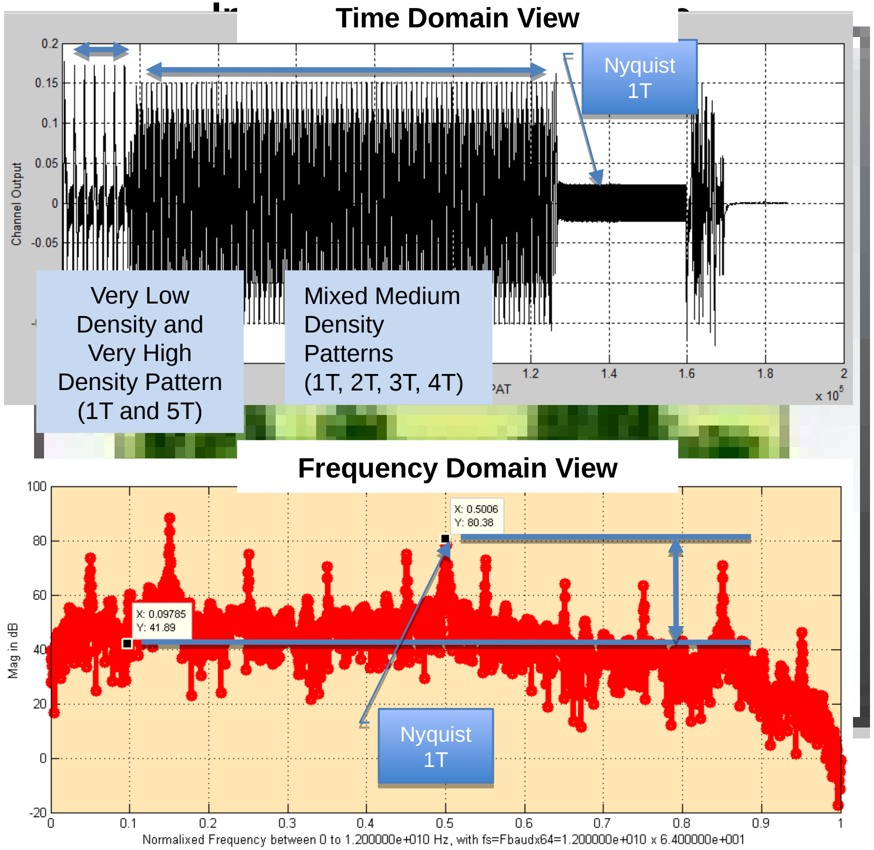
- In nanometer circuit design, with increased transistor density, device self heating changes its operating state
- Device startup temperature during initial training may be very different from device steady state operation
  - Temperature difference effects MOSFET threshold voltage, electron mobility, leakage, and thermal conductivity
- SerDes gain and boost changes between initial and final temperature deviation requires re-tuning of receiver parameters
- An example Gm and Ron variation over temperature is shown to be not insignificant



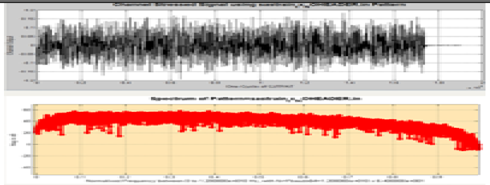
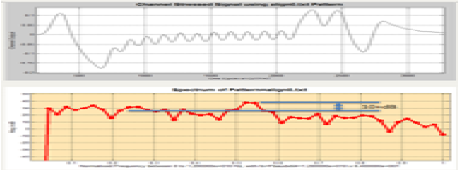
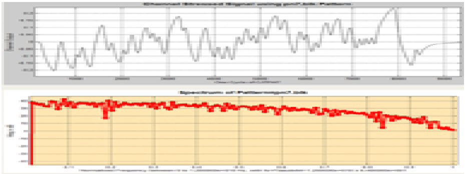
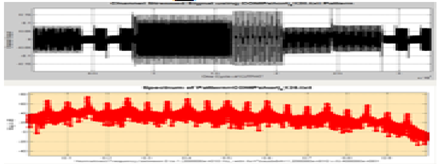
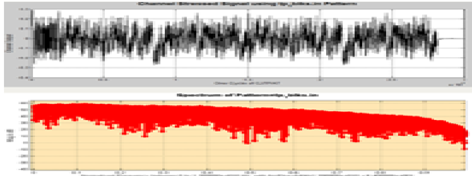
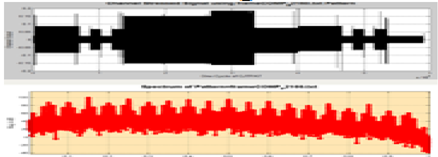
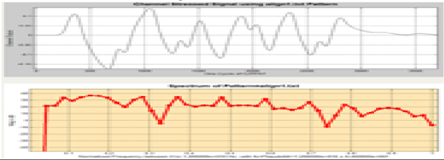
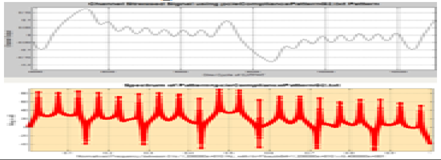


Time and Frequency Domain View of Pattern Characteristics

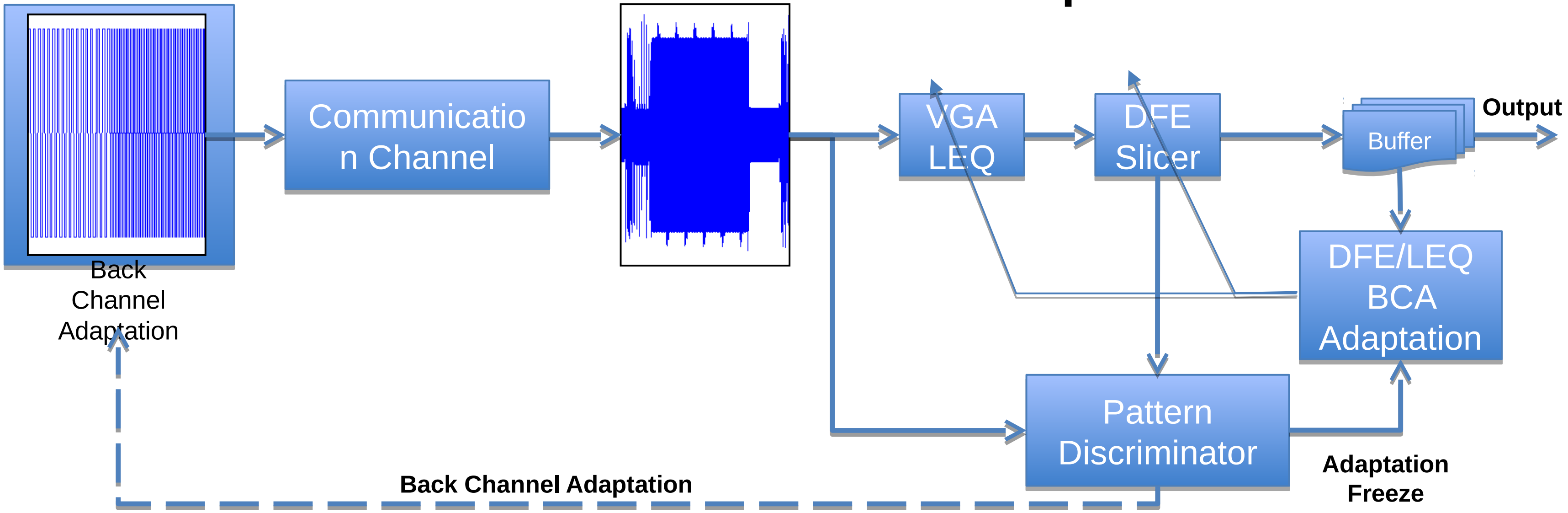
- A key to good adaptation relies on the availability of spectrally rich pattern at the receiver
- In absence of good spectral content in a pattern the receiver operating margin degrades
- The CJTPAT is a popular stress pattern used in SerDes evaluation
- A time domain view of CJTPAT
  - After passing a CJTPAT through a high loss channel, the contents of CJTPAT is revealed
  - Long string of 1010 (1T) pattern suffers most loss
  - Mixed tone (1T, 2T, 3T, and 4T) patterns consists of a large block of CJTPAT
  - The mostly 1T and 5T patterns are at the beginning
  - An intuitive feel can be achieved from time domain view for the CDR impact and adaptation impact
- A frequency domain view of CJTPAT
  - The frequency contents of the CJTPAT is revealed in the FFT output



Spectral Contents of Some Commonly Used Patterns

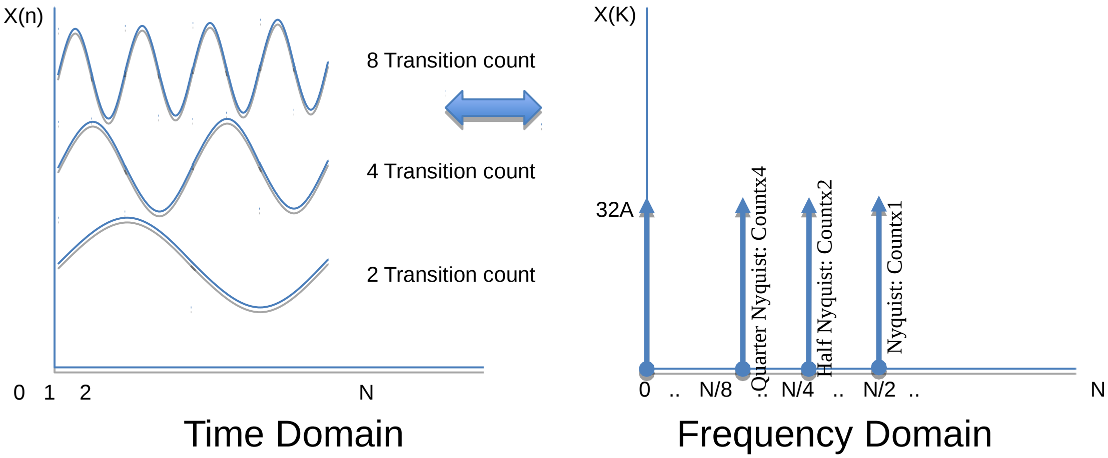
PATTERNS FAVORABLE TO SERDES OPERATION; PATTERNS WITH GOOD SPECTRAL CHARACTERISTICS	PATTERNS DETRIMENTAL TO SERDES OPERATION; PATTERNS WITH POOR SPECTRAL CHARACTERISTICS
SASTRAIN	Align0 Pattern
	
PN7 	COMP_short Patten 
TP1 Pattern 	Frame Comp Pattern 
Align1 Pattern (less than Reasonable) 	PCIE Compliance Pattern G2 

Pattern Discriminator Assisted Adaptation



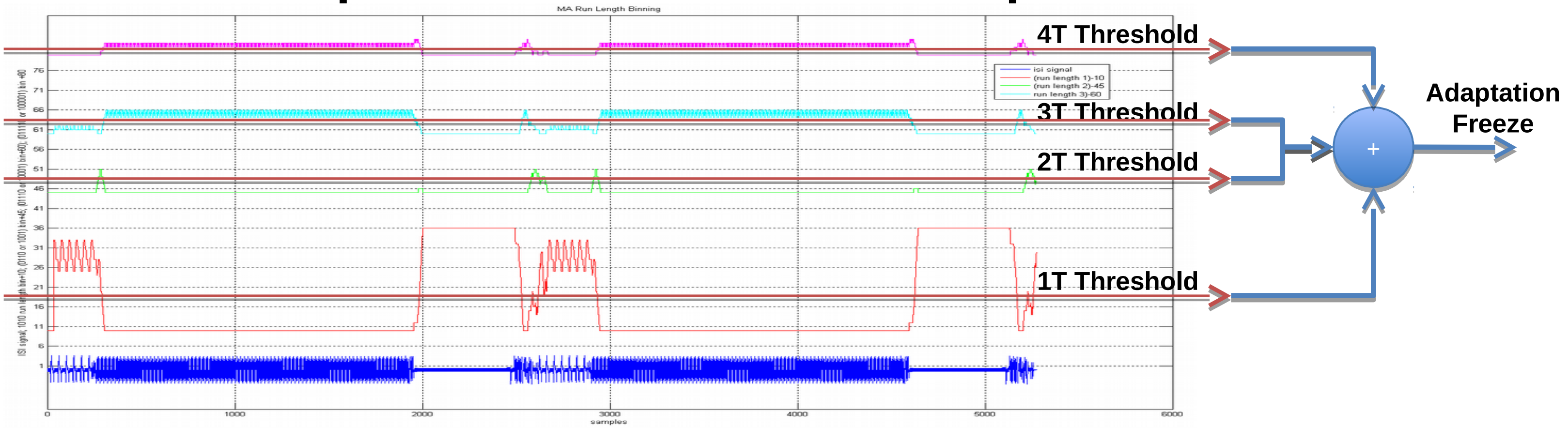
- Adaptation over a tone like pattern will mis-tune the transceiver
- Operating a CDR over a tone like pattern will shift optimal sampling phase
- A solution to preserving the transceiver integrity requires a pattern discriminator
  - Inhibit adaptation over tone rich pattern
  - Resume adaptation with a delay after tone recedes (allow phase to resettle)

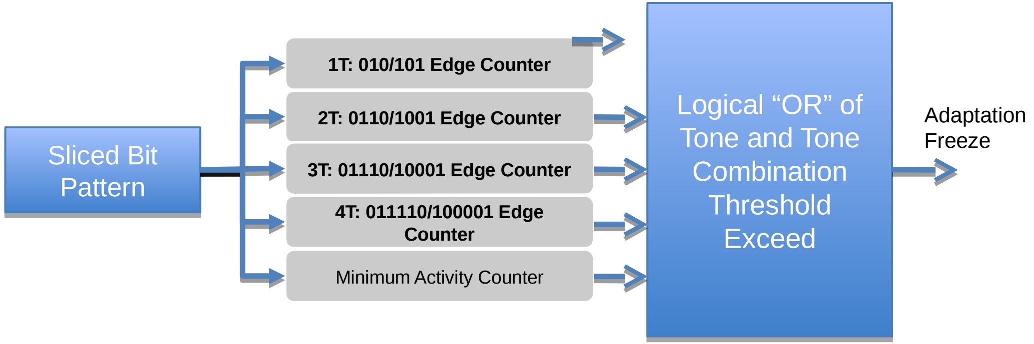
Tone Discriminator Equivalence to FFT



- The pattern discriminator essentially works as magnitude response of FFT
- Consider a block with N input bits
  - If it has N 0to 1 or 1 to 0 transitions then the block represents a Nyquist tone
  - If it has N/2 110 or 001 transitions, then the block represents a half Nyquist tone
  - A combination of tone transition count will give other frequency components

An Example Pattern Discriminator Operation on CJTPAT

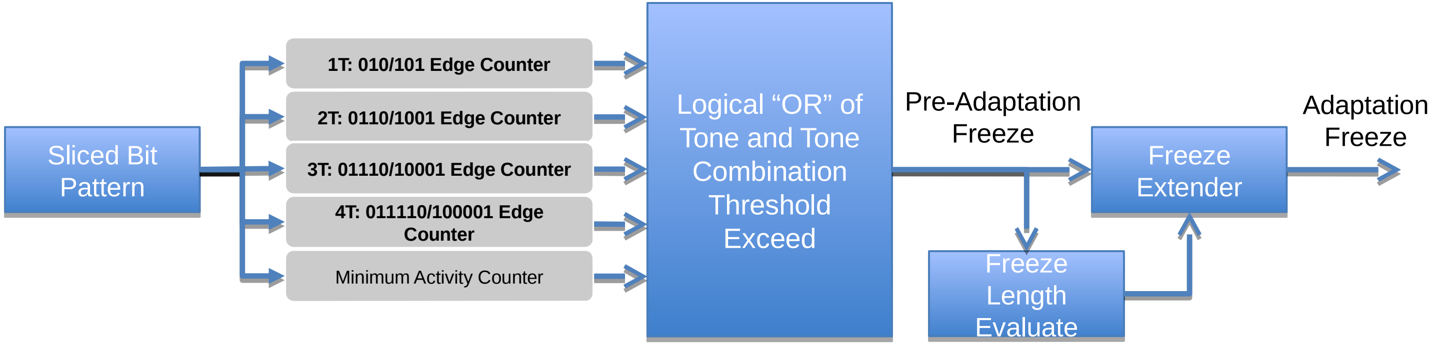




- A 1T detector counts all 010 and 101 transition and peaks over 1T block
- Similarly 2T (1001, 0110 transition), 3T (01110, 10001) , 4T (011110, 100001) detectors peaks at other segments on CJTPAT
- When any tone exceeds a programmable threshold, the output adaptation freeze is asserted telling adaptation blocks not to use those bits for adaptation

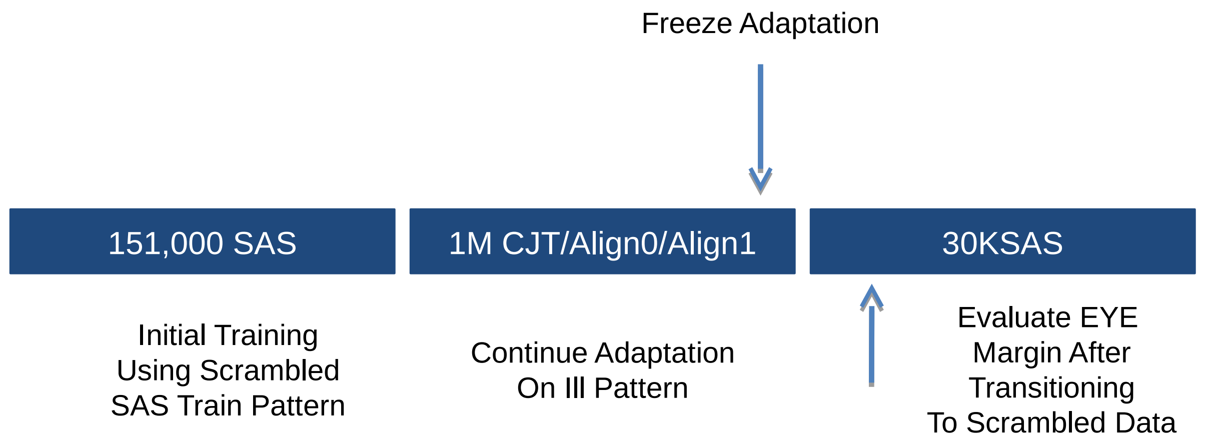
Pattern Discriminator Architecture

- The pattern discriminator operates on a N-bit block of bits
- It overlaps on N/2 bits on earlier block
- It has parallel counters for 1T, 2T, .., mT bit run length
- Each run length counter has a corresponding count threshold
- If any of the count exceeds their set threshold then the entire N bit data is eliminated in adaptation
- If the tone persisted for an extended period, the CDR phase has drifted and adaptation error information is skewed. To allow CDR to re-center, extend the adaptation freeze longer



Pattern Discriminator Assisted Adaptation

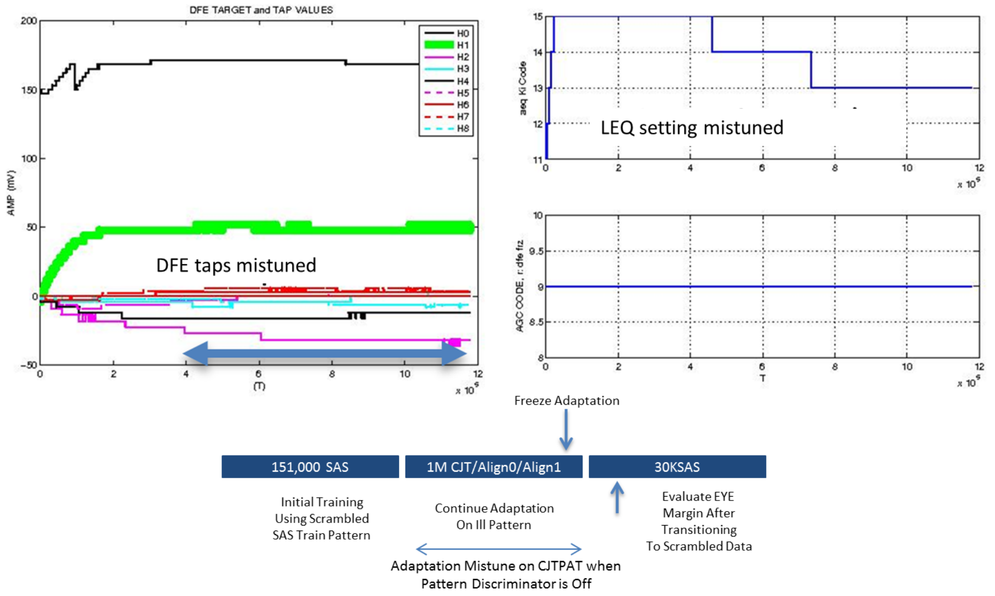
- The effectiveness of the pattern discriminator assisted adaptation operation is evaluated using following pattern design



- Initially 151K scrambled SAS train pattern is used for transceiver tuning
- Next 1 million ill pattern is sent in (SAS/SATA Align0 or Align1, or CJTPAT).
  - In one case the pattern discriminator (PD) is turned on and in another case the PD is turned off
- At the end of the ill pattern all adaptation is frozen.
- Next Another 30K bits of scrambled SAS train pattern is used to measure receiver EYE height and width

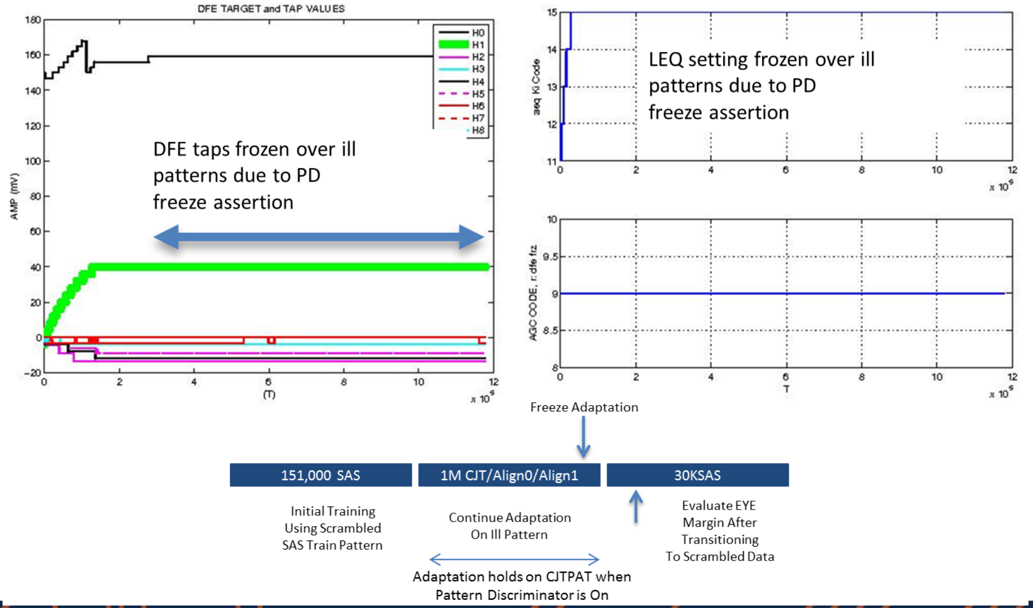
Pattern Discriminator Assisted Adaptation – PD Off Case

- The initial receiver training was done with scrambled 151K SAS train pattern over a 10m iPASS cable
- Next 1M CJTPAT bit is used with PD turned off. The linear equalizer boost started to drop on CJTPAT, the DFE taps (specially H2 over this particular channel) started to build up to more negative value
- At the end of the CJTPAT pattern the receiver EYE opening is measured using SAS train pattern
- Over CJTPAT the RX was mistuned resulting in
  - Degraded EYE margin
-



Pattern Discriminator Assisted Adaptation – PD On Case

- The initial receiver training was done with scrambled 151K SAS train pattern over a 10m iPASS cable
- Next 1M CJTPAT bit is used with PD turned on. The linear equalizer boost remained frozen on CJTPAT, the DFE taps remained unchanged due adaptation suppression
- At the end of the CJTPAT pattern the receiver EYE opening is measured using SAS train pattern
- Over CJTPAT the RX was not mistuned resulting in
  - EYE margin is preserved



SAS/SATA/FC 8b/10b Pattern Evaluation with PD – Long Channel

- Test Case 1: Turn off pattern discriminator. Perform initial adaptation on 151K UI SAS scrambled data pattern, then continue to adapt on 1M UI pathological pattern and freeze adaptation then switch to 30K UI scrambled data to measure EYE margin.
  - Performance significantly degrades without PD on pathological pattern
- Test Case 2, 3, 4, 5, 6: Same as test case 1, but turn on pattern discriminator constrained adaptation.
  - With PD on the performance is preserved closer to initial adaptation results

PATTERN DISCRIMINATOR EVALUATION ON LONG CHANNEL USING CJTPAT AS THE PATHOLOGICAL PATTERN.

Adaptation with scrambled pattern		Adaptation continue on CJTPAT with PD off		Adaptation continue on CJTPAT with PD on	
VM	HM	VM	HM	VM	HM
89	0.63	9.7	0.25	66	0.50

Pattern discriminator evaluation on long channel using ALIGN1 as the pathological pattern.

Adaptation with scrambled pattern		Adaptation continue on ALIGN1 with PD off		Adaptation continue on ALIGN1 with PD on	
VM	HM	VM	HM	VM	HM
89	0.63	42	0.32	71	0.53

Pattern discriminator evaluation on long channel using frameComp as the pathological pattern.

Adaptation with scrambled pattern		Adaptation continue on frameCOMP with PD off		Adaptation continue on frameCOMP with PD on	
VM	HM	VM	HM	VM	HM
89	0.63	35	0.41	72	0.56

SAS/SATA/FC 8b/10b Pattern Evaluation with PD – Short Channel

- On short channel performance degrades significantly without PD on
- With PD on the performance remained very close to initial adaptation with scrambled data

Pattern discriminator evaluation on short channel using CJTPAT as the pathological pattern.					
Adaptation with scrambled pattern		Adaptation continue on CJTPAT with PD off		Adaptation continue on CJTPAT with PD on	
VM	HM	VM	HM	VM	HM
102	0.56	73	0.44	105	0.56
Pattern discriminator evaluation on short channel using COMP_Framed_RD as the pathological pattern.					
Adaptation with scrambled pattern		Adaptation continue on COMP_Framed_RD with PD off		Adaptation continue on COMP_Framed_RD with PD on	
VM	HM	VM	HM	VM	HM
102	0.56	78	0.41	103	0.56
Pattern discriminator evaluation on short channel using frameCOMP as the pathological pattern.					
Adaptation with scrambled pattern		Adaptation continue on frameCOMP with PD off		Adaptation continue on frameCOMP with PD on	
VM	HM	VM	HM	VM	HM
102	0.56	69	0.41	101	0.56

PCIe Gen3/Gen4 and SAS4 Evaluation with PD

- Unlike in 8b/10b patterns, emerging SAS and PCIe standard uses PN23 scrambled data
- Performance of PCIe Gen4 16GT/s on a 28dB channel and SAS4 24Gbps on a 30dB channel is evaluated with
  - PD turned on
  - PD turned off
- No significant performance difference was observed with PD on in PCIe Gen4 and SAS4 application

TX SETTING	NO PATTERN DISCRIMINATOR		PATTERN DISCRIMINATOR	
	VOLTAGE MARGIN MVP	JITTER MARGIN UIPP	VOLTAGE MARGIN MVP	JITTER MARGIN UIPP
SAS4 TX no Emphasis	70mVp	0.406UIpp	66mVp	0.406UIpp
SAS4 TX with 2.5dB Pre-Emphasis	81mVp	0.5UIpp	87mVp	0.5UIpp
PCIE4 TX no Emphasis	121mVp	0.56UIpp	116mVp	0.68UIpp
PCIE4 TX with 2.5dB Pre-Emphasis	112mVp	0.53UIpp	116mVp	0.59UIpp

Conclusion

- Temperature, humidity, and slow voltage variation over time is inevitable that renders initial adaptation values not optimal at prolonged steady state operation.
- Periodic adjustment to receiver equalization parameters is necessary for maintaining good operating noise and jitter margin.
- But good scrambled data pattern is not guaranteed in mission mode of operation carrying live traffic in traditional 8B/10B SAS/SATA application.
- This paper offers a method and apparatus to detect presence of pathological pattern that are not favorable for adaptation and allows a constrained transceiver adaptation only when presence of spectrally rich pattern is detected.
- We evaluate the PCIe Gen4 and SAS4 performance with and without pattern discriminator using a 28dB channel @8GHz and 30dB channel @12GHz respectively. Results show that no significant difference with and without pattern discriminator due to use of PN23 pattern in emerging SAS4 and PCIe Gen4 application