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SerDes Steady State Adaptation Challenges in Existing SAS/SATA and Emerging PCIe Gen4/SAS4 Application and their Solutions with Pattern Discriminator Constrained Adaptation

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Abstract

In PCIe/SAS/SATA application, steady state adaptation is required to track changes in channel characteristics due to changes in ambient temperature and humidity. As a result,

voltage, temperature, and humidity (VT-humidity) induced changes in the system characteristics renders initial training obsolete over time. In storage-standards-based applications, there is no guarantee for scrambled data on the wire. As a result, if unconstrained steady state adaptation is performed on pathological patterns with poor spectral content, the SerDes receiver can potentially mistune its adaptation parameters and introduce BER. This paper introduces a pattern discriminator to block adaptation when pathological patterns are detected and allows proper adaptation when spectrally rich patterns are present on the line.

Author(s) Biography

Mohammad S. Mobin earned his PhD in electrical engineering from Southern Methodist University in 1992. He also holds MSEE and BSEE from University of South Alabama and Bangladesh University of Engineering and Technology. He joined AT&T Micro-electronics in 1992 which subsequently spun out to Lucent Technologies, Agere Systems, merged in to LSI Corporation and finally acquired by Avago Technologies. During last 22 years he was involved with DSP1600 and DSP16000 series Architecture definition, GSM system solution, DSP embedded Viterbi algorithm hardware accelerators, convolution decoders, MLSE channel equalization, pre-amplifier linearization techniques, cable modem transceiver design, SONET add/drop multiplexer design and definition. In last ten years M. S. Mobin is involved with SerDes architecture definition, system modeling and simulation. He is deeply involved with channel equalization and timing recovery techniques. Currently he is a distinguished engineer at Avago Technologies. He has 89 US patents granted in his name; he published various papers in IEEE transactions in Biomedical Engineering, and other conferences.

Amaresh Malipatil is currently a Senior Principal Engineer at Rambus Inc. in Sunnyvale, CA. Prior to this; he was a SerDes architect and manager at LSI Corp. in Milpitas, CA. He received his Bachelor of Engineering degree in Electronics and Communications Engineering from National Institute of Technology Karnataka, India in 2001. He received his Master of Science and Ph. D. in Electrical Engineering from University of Notre Dame. He is involved in developing system architectures for high speed SerDes. His research interests are in the field of signal processing and communications over high speed links including link analysis, equalization, clock-and-data recovery, as well as linear and nonlinear signal processing with applications in wireless communications, distributed signal processing over sensor networks.

Sunil Srinivasa received his Ph.D. degree from the department of Electrical Engineering at University of Notre Dame, Indiana in 2011. Since 2011, he has been employed as a Senior Systems Design Engineer at Avago Technologies (previously LSI Corporation), and is involved in developing leading-edge high-speed Serdes system architectures. Prior to this, he received the B. Tech degree in electrical engineering from the Indian Institute of Technology, Madras, India (IITM) in 2004 and the M.S. degree in electrical engineering from the University of Notre Dame, Indiana in 2007. His specialties include

signal processing and communication over high-speed serial links (SerDes), wireless communications and networking and stochastic geometry.

Weiwei Mao received his Ph.D. in electrical engineering from University of Colorado at Colorado Springs in 1991. He also received his M.S.E.E. and B.S.E.E. from Fudan University, China. He is currently a principal engineer at Avago Technologies working on mixed-signal design of SerDes transceiver. In 1996, He joined Lucent Technology which spun out to Agere Systems, later merged with LSI Corporation which was acquired by Avago Technologies. He was also a principal/senior member of engineering at Ford Microelectronics, Inc. from 1990 to 1996.

Dr. Haitao (Tony) Xia is Senior Manager of R&D at Avago Technologies, leading the research and development of advanced read channel and Serdes architectures for data storage systems. Dr. Xia is the current Chairman of IEEE Data Storage Technical Committee and President of Chinese American Information Storage Society (CAISS). Before his work at Avago/LSI, Dr. Xia worked at Silicon Valley start-up, Linked-A-Media Devices, on signal processing and coding in the area of magnetic recording channels and non-volatile memories. Dr. Xia has published more than 20 articles in peer-reviewed journals/conferences, and has more than 50 US patent granted to his name. Dr. Xia is an IEEE Senior Member.

Aravind Nayak is a principal engineer with Avago Technologies in Allentown, PA. He holds PhD (2004) and MS (2000) degrees in electrical engineering from the Georgia Institute of Technology, Atlanta, GA, and B. Tech (1999) degree in electrical engineering from the Indian Institute of Technology, Madras, India. His research interest include signal processing for the magnetic recording read channel and SerDes applications.

Introduction

Temperature, humidity, and voltage effect on channel loss, phase spread, and silicon gain, boost, and BW

Impact of channel and silicon characteristics changes, (over time initial adaptation is not optimal for prolonged steady state operation without retuning

Problems with patterns

How to overcome the problem using pattern discriminator

TBD

Ambient Factors Effecting Channel Characteristics

The transmission line offers frequency selective losses on the signal transmitted through it. The dominant losses exerted by the transmission line falls under following categories:

1. Low frequency losses when current is uniformly distributed in conductor cross section
2. Frequency dependent conductor losses
3. Frequency dependent dielectric losses
4. Loss due to surface roughness

Physics of Frequency Dependent Conductor Losses

Low Frequency Conductor Loss

At lower frequency electrical resistance is a function of,

$$R = f\left(\frac{L}{A}\right) = \rho\frac{L}{A}$$

Where, L=Length of the trace, A is the cross section area through which current flows, and ρ is a temperature dependent resistivity of the material. It is a function of other variables as shown below [1],

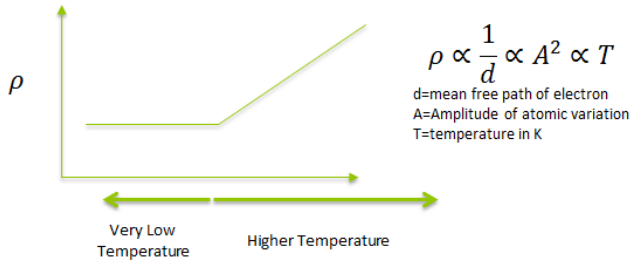


Figure 1 Resistivity behavior at high and low temperature

Source: http://hyperphysics.phy-astr.gsu.edu/hbase/electric/restmp.html#c1

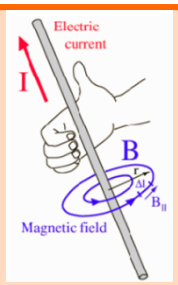
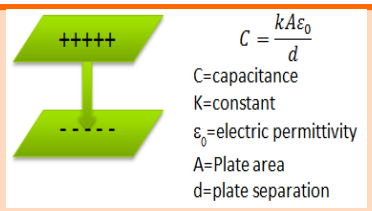
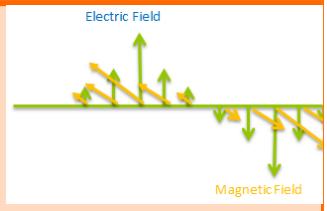
High Frequency Conductor Loss

As frequency increases through conductor magnetic fields vector, B, are produced by the flow of electrons [2] as shown in Table 1, where B is the magnetic field, I is the current flow, r is the radius of the field, and μ is the permeability.

The electric field vector, E, emerges from a positive point charge to a negative point charge, expressed as $E = \frac{F}{q}$, where F is the electric force vector expressed in Newton (N) and q is the charge in coulomb[3].

The above mentioned electric and magnetic fields are orthogonal to each other.

Table 1: Basic Field properties

Magnetic Field	Electric Field	Orthogonal Electric and Magnetic Field
 **Source: http://hyperphysics.phy-astr.gsu.edu/hbase/magnetic/magcur.html#c3** **Magnetic field due to current flow**	 Electric field and Capacitance from parallel plates	 Orthogonal relationship between electric and magnetic fields

The current through a conductor creates magnetic field, and the magnetic field in turns creates Eddy current. Eddy current direction inside conductor is in the opposite direction of the primary current and hence reduces the current density inside the conductor core. While the Eddy current away from the conductor core is in the same direction as the primary current, hence reinforces current at the surface. This creates skin effect in current carrying conductor at high frequencies [4].

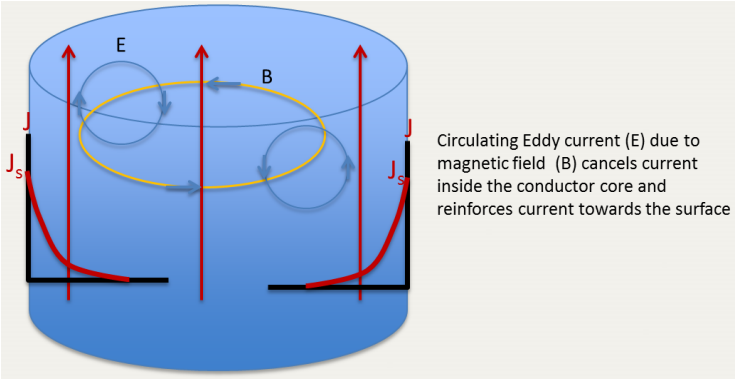


Figure 2: Skin effect principle

Source: http://hyperphysics.phy-astr.gsu.edu/hbase/electric/skineffect.html , http://en.wikipedia.org/wiki/Skin_effect

As a function of signaling rate, the current density denoted as J is the maximum at conductor surface and exponentially decays inside the conductor following [4],

$$J(T,f) = J_s e^{\left(\frac{-d}{\delta}\right)}, with\ \delta = \sqrt{\frac{2\rho}{w\mu_r\mu_0}} \propto \frac{T}{\sqrt{f}}$$

Where,

$J_s = current\ density$,

$d = depth$ ¿ $surface$,

$\delta = skin\ depth\ where\ current\ is\ \frac{1}{e}\ of\ the\ surface$,

$\rho = resistivity\ of\ the\ conductor$,

$\omega = 2\pi f\ is\ the\ angular\ frequency\ of\ the\ signal$,

$\mu_r = relative\ magnetic\ permeability\ of\ the\ conductor$,

$\mu = permea\ bility\ at\ vacuum\ .\ ,J$

If conductor thickness is larger than skin depth, the AC resistance increases by $\sqrt{f}$ [13-14]

With increasing temperature the resistivity increases and the skin depth increase

Frequency Dependent Dielectric Losses

Traces in the PCB are filled with polar molecules with random orientation. In presence of signaling the induced electric field will polarize the dielectric polar molecules. This decreases the effective electric field between the plates. The capacitance is inversely proportional to the electric field. Effective electric field being less than the applied electric field results in increase in the capacitance between the parallel plates [5].

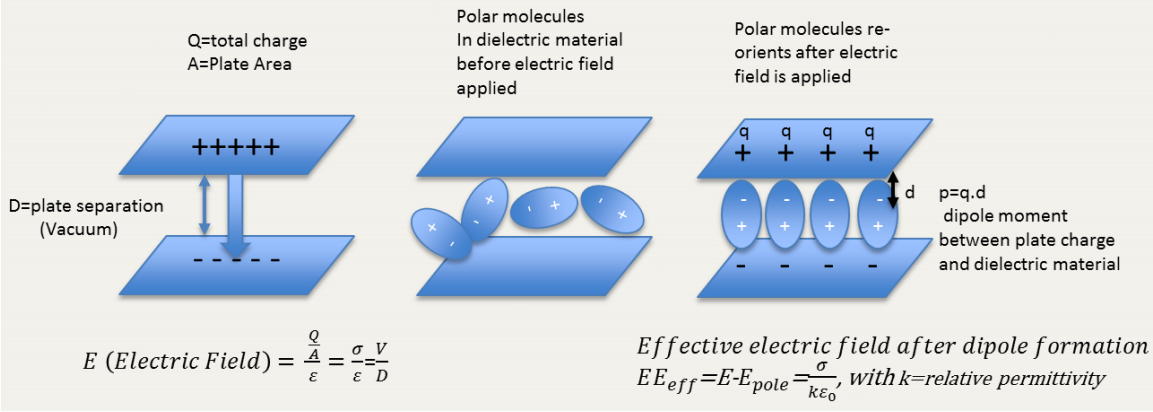


Figure 3: Dielectric dipole orientation with electric field

As the signaling speed increases, the orientation of the dielectric field changes. This constant orientation and reorientation dissipates energy. At high, speed dielectric loss between conducting plates has a dominant share of channel loss. The electrical model of such imperfection consists of a capacitor with a perfect dielectric in parallel with a resistor to account for the loss component as shown in Figure 4. Here the resulting current consists of 90^0 capacitive current with an in-phase resistive current. The small

angle, δ, between the resulting current with the capacitive current is termed as the dielectric loss angle, and the term tan(δ) is the dissipation factor of the dielectric.

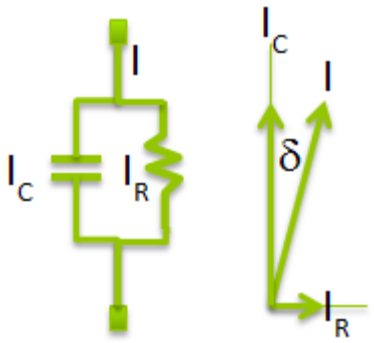


Figure 4: Equivalent circuit for lossy dielectric

The relative permittivity (a.k.s. dielectric constant) of commonly used PCB materials can vary up to 5% over 50Ω above room temperature, while the dissipation factor can vary close to 40% over the same temperature range. Variations in temperature and humidity increases change the dielectric loss property [6-7].

The dielectric loss is a strong function of temperature and humidity

Loss Due to Surface Roughness

Surface roughness is essential for attaching traces with PCB, but detrimental to channel loss at high frequencies when skin depth is comparable or less than surface roughness. At very high frequencies when most of the current travels through the skin of the conductor, surface roughness increases the effective length of the electrical path and hence electrical loss [14].

Resistivity increases with temperature and hence loss due to surface roughness increases with temperature

Quantitative Impact of Channel Loss Parameters

After establishing the temperature dependent channel loss parameters, we next show the impact of their variation on channel loss and the state of signal quality. We model a simple channel consisting of a MICROSTRIP, a VIA to route signal to an internal layer, a STRIPLINE in the internal layer, a VIA to route signal back to top layer, and finally a MICROSTRIP to the end point as shown in Figure 5.

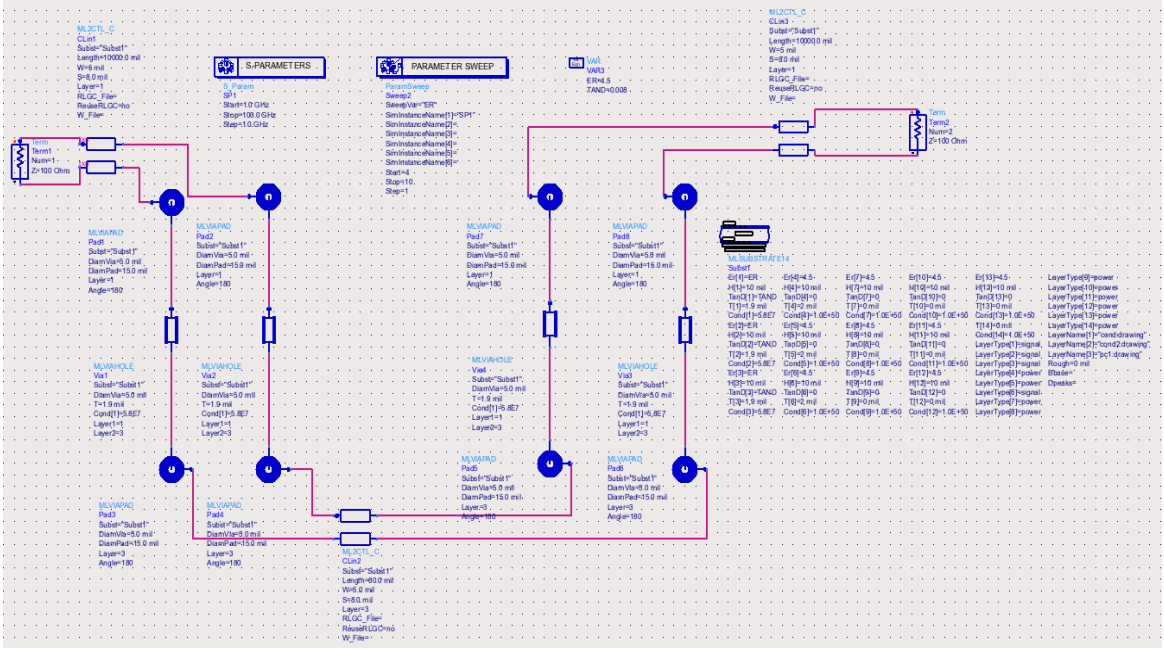
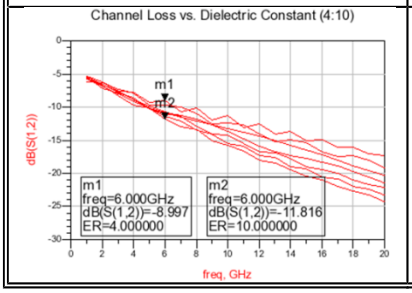
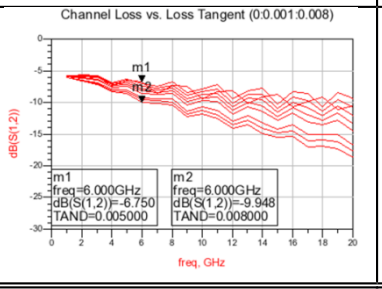
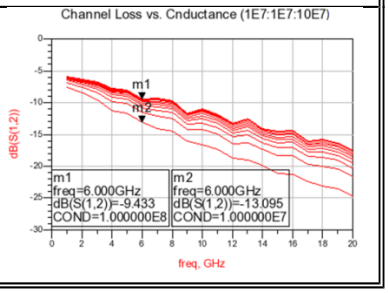


Figure 5: An example channel model to evaluate channel loss variation due to PCB material characteristics variation

In this study a parametric sweep of the relative permittivity of the dielectric material, the conductance of the traces, and the loss tangent is performed in above test bench. The simulated channel loss variation is tabulated in Table 2.

Table 2: Impact of channel characteristics variation on channel loss

CHANNEL LOSS VARIATION DUE TO RELATIVE PERMITTIVITY VARIATION BETWEEN 4 TO 10	CHANNEL LOSS VARIATION DUE TO DIELECTRIC LOSS TANGENT VARIATION BETWEEN 0.001 TO 0.008	CHANNEL LOSS VARIATION DUE TO CONDUCTANCE VARIATION BETWEEN 1E7 TO 10E7
		

We configured the schematic in Figure 6 so that channel loss parameters are grouped to offer the worst case loss and the best case loss using the boundary parameters used in table 2. A transmitter running at 8Gbps is applied at channel input and on the receive side

a passive linear equalizer is used to open the EYE with the upper bound of the channel loss using above loss parameter combination. Then the lower bound of the channel loss is configured to show the EYE distortion due to channel loss variation.

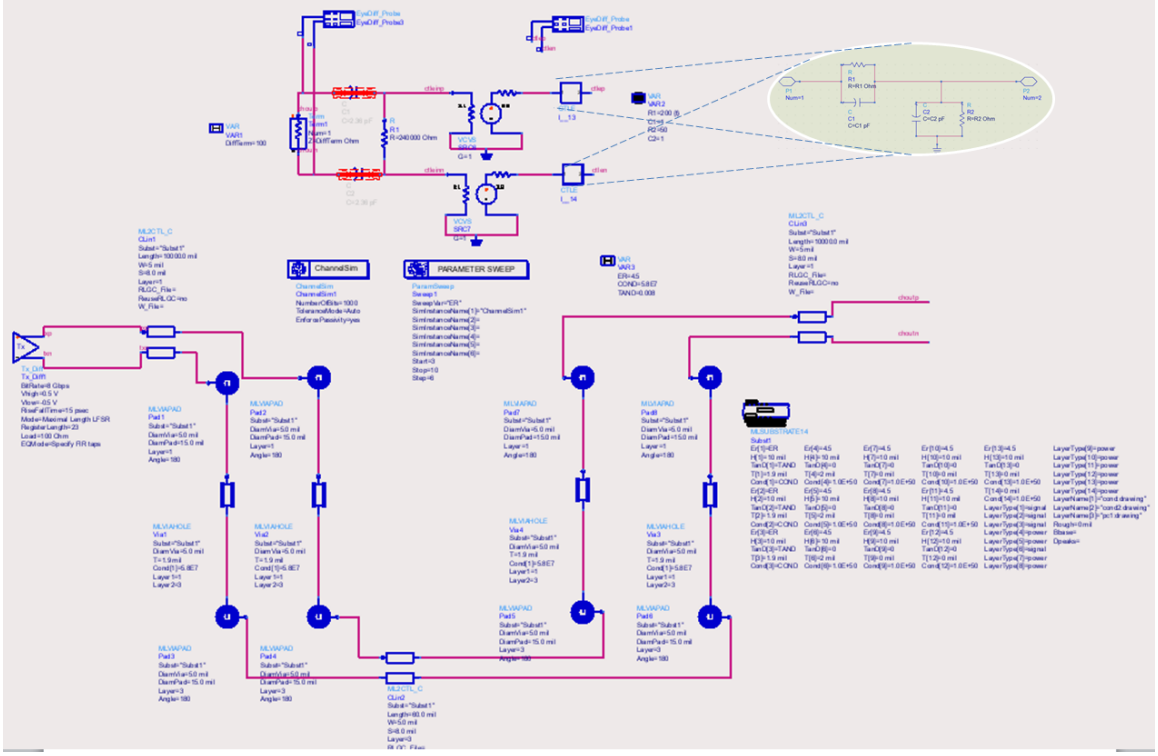
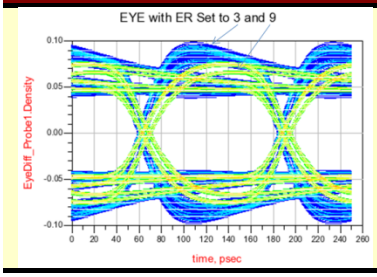
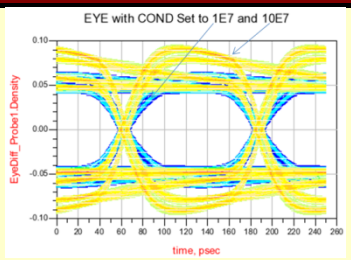
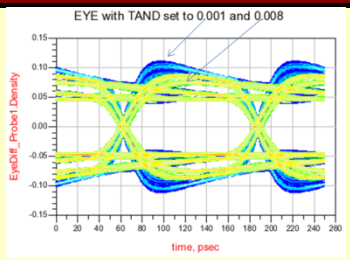


Figure 6: EYE quality evaluation simulation setup between the worst and best case channel loss

The EYE diagram for the worst case channel loss is overlaid on the EYE diagram for the best case channel loss. The results are tabulated in Table 3.

Table 3: Channel loss contributing parameter change effect on EYE

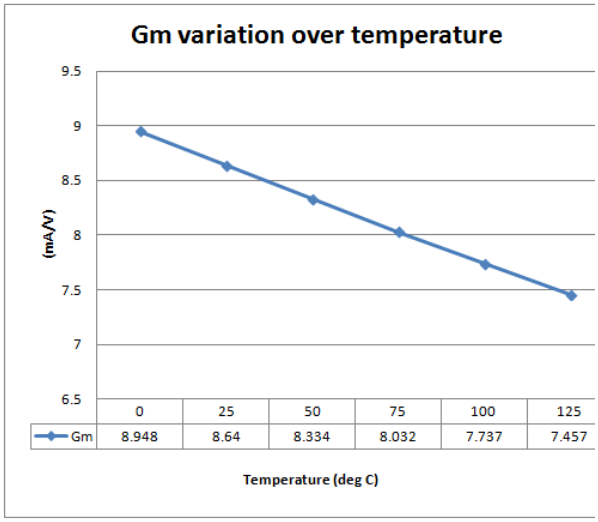
EYE by setting dielectric constant to 3 and 9	*EYE by setting conductance to 1E7 and 10E7*	*EYE by setting loss tangent to 0.001 and 0.008*
		

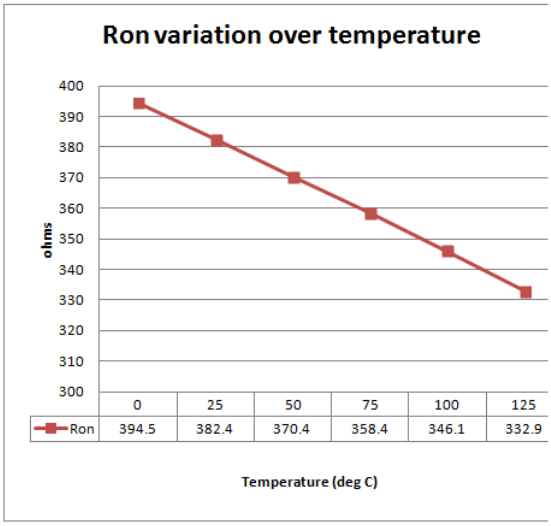
Sensitivity of semiconductor devices to voltage and temperature (VT) variation and its effect on Gm, circuit gain and bandwidth

In nanometer circuit design the effect of device self-generated heating becomes more and more pronounced as the density of the transistors continue to increase. The large variation of device temperature is expected in different operation states. For example, the temperature of a device at power up may be significantly different from the one in a steady state operation. The power up and power down scheme may also affect the temperature at different circuit regions. The variation of device temperature will affect mosfet threshold voltage, electron mobility, leakage, and thermal conductivity, etc. Therefore, it will affect SerDes performance caused by the temperature induced variation of the gain, boost, bandwidth, clock skew, clock duty cycle, etc.

With increasing technology shrinks the PVT variation is becoming more dominant. The PVT variation manifests itself as variations in $gm=\frac{\delta I_D}{\delta V_{GS}};$ which can be represented in various forms, $gm=\mu C_{ox}\frac{w}{L}(V_{GS}-V_{th})$, or $gm=\frac{2I_D}{V_{GS}-V_{th}}$, where $I_D=\frac{1}{2}\mu_n C_{ox}\frac{W}{L}V_{GS}-V_{th}¿^2$. It is evident that variations in W, L, μ, Vgs, Vth over PVT corners will create variations in gm.

In SerDes Rx data path, resistive load CML style amplifiers are widely used. For a typical resistive load CML amplifier, the small signal dc gain is Av=gm*(RL||Ron), where RL is the load resistance. At worst case fast corner, i.e. FFF, RL has the low resistance. Both gm and Ron will be reduced over temperature significantly to result in a minimum gain Av at this corner. The following simulation results show the gm and Ron variation over temperature for a typical 28nm data amplifier.





Temperature dependence on Gm and Ron

The following two tables show gm/Ron reduction of each stage of an Rx data path when temperature changes from 0C to 125C. A generic data path is used in current simulation where various stages are termed as Block1:4 in a generic manner

Gm	0	125	Gm reduction (dB)
Block 1 (mA/V)	24.09	20.23	-1.52
Block 2 (mA/V)	5.835	5.031	-1.29
Block 3 (mA/V)	18.23	15.63	-1.34
Block 4 (mA/V)	8.948	7.457	-1.58

Ron	0	125	Ron reduction (ohms)
Block 1 (ohms)	153.6	121.9	-2.01
Block 2 (ohms)	734.2	644.8	-1.13
Block 3 (ohms)	248.9	230.1	-0.68
Block 4 (ohms)	394.5	332.9	-1.47

In SerDes receiver *gm* variation in various data path blocks creates an accumulated composite gain variation. Such data path gain variation impacts the system BER

performance unless a re-adaptation is done to re-optimize the receiver adaptation parameters.

Effect of Ambient Condition Changes on Signal Quality

With increasing link speed SerDes unit interval (UI) is decreasing while channel loss support requirements are increasing. In 6G SAS2, with 166ps UI, most practical application supported 20+ dB insertion losses at Nyquist, while 12G SAS3, with 83.3ps UI, supports 24dB insertion loss at Nyquist, while evolving 20G/24G SAS4 application is targeting for 30dB channel loss at Nyquist at the ball. Similar increasing channel loss trend is also observed in PCIe Gen3 to PCIe Gen4 application as the standard for PCIe Gen4 is evolving at the moment. Because of challenges associated with signal quality with high speed high loss application, standards are offering a training state at the beginning of link acquisition, so that transmitter and receiver can jointly train their equalization parameters [8]. During training period spectrally rich training patterns are used for adaptive tuning of transceiver parameters.
After initial training if the operating ambient temperature and humidity condition changes then channel characteristics also changes. The channel characteristics also changes due to changes in external board/backplane as well as die characteristics changes. An exemplary qualitative channel loss profile changes is presented in Figure 7.

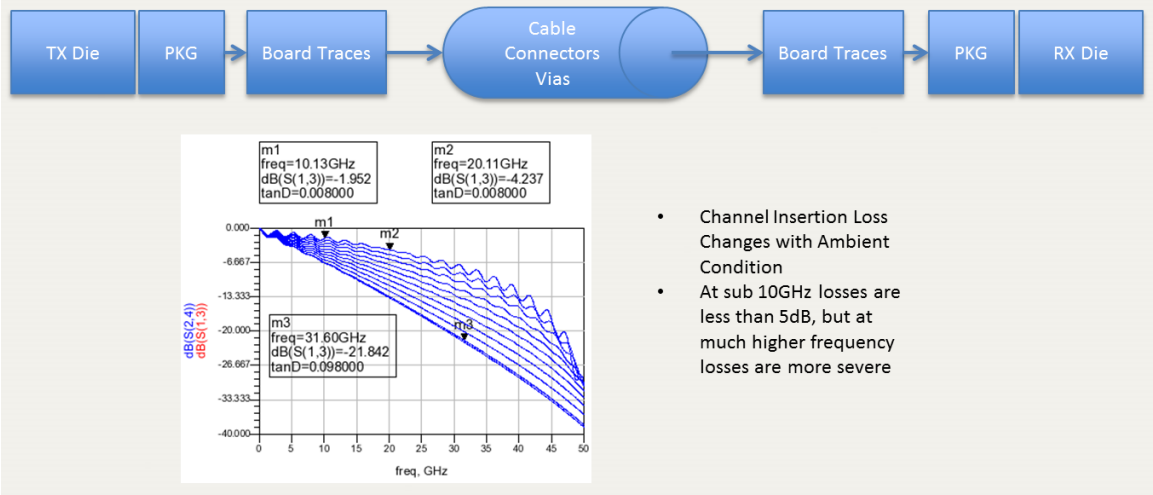


Figure 7: Channel loss changes due to board/backplane/connector/via and die characteristics changes

To overcome signal quality degradation due to channel loss changes with ambient condition, the transceiver needs to re-adapt its adaptation parameters. If re-adaptation is not performed, the transceiver will operate with reduced noise and jitter margin. An exemplary initial transceiver optimized EYE at the input to the slicer is presented in Figure 8. In this case the initial EYE opening was 150mV peak to peak and the horizontal EYE opening was 0.8UI peak-peak for a 19.9dB insertion loss at Nyquist. The

equalization offered 11.7dB gain at Nyquist, and the resulting equalized signal had -7.7dB gain at Nyquist. In this simple experiment the equalization contribution from decision feedback equalizer was not used.

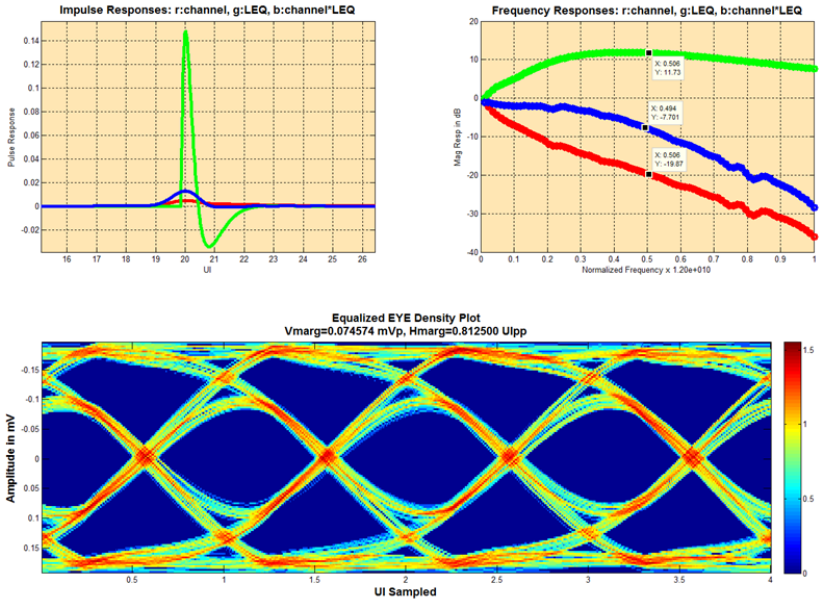


Figure 8: Adaptation and signal quality after initial adaptation

No existing standard offers periodic retraining pattern and does not guarantees spectrally rich steady stream of pattern for short term periodic adaptation. If a receiver periodically wakes up for readapting its equalization parameters, it may do so on link management patterns that are often non scrambled, such as clock tolerance skip-order-set (SOS) pattern in PCIe [9] or ALIGN1 pattern in SAS application [10], just to name a few. In absence of any pattern discriminator assisted adaptation scheme a receiver will not attempt to adapt on spectrally poor patterns even when channel characteristics changes with changes in ambient condition. To emulate the consequences of not readapting the equalization parameters in following experiment the channel loss is increased by 3.65dB at Nyquist in line with measurement data [7]. In this case, as shown in Figure 9, both noise and jitter margin is reduced to 88mV peak-peak and 0.75UI peak-peak. Where at Nyquist the initial channel loss was 22.8dB and the linear equalizer offered 11.35dB and the resulting equalized signal had -11.35dB gain at Nyquist. For an approximate -3.65dB excess gain in the channel the vertical EYE margin loss is in par with expected loss 150*(10^(-3.65/20))=98mV. The 10mV difference between calculated EYE closure and simulated EYE closure is attributed to ISI contribution from other frequency points.

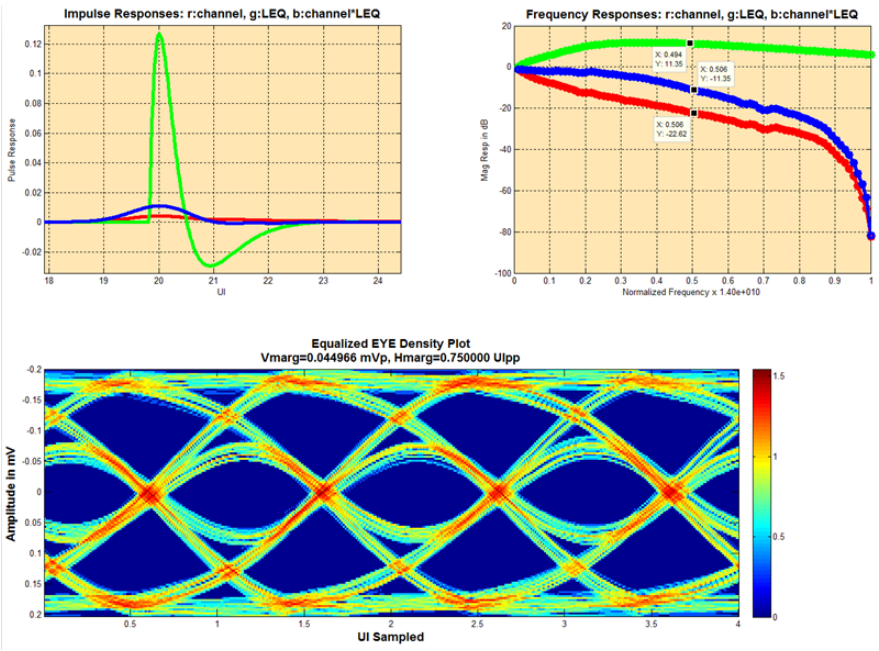


Figure 9: Degraded EYE quality witch changes in ambient condition without re-optimizing the transceiver

The loss in performance with channel characteristics variations can be recouped if the pattern is random enough or if there is a means to suppress nonrandom patterns from incoming bit stream on which re-adaptation can be performed as long as the transceiver has enough equalization range. In this paper we present a method and apparatus to perform pattern discrimination such that adaptation is turned on only on random patterns and adaptation is suppressed on non-random and tone dominated patterns.

Spectral Characteristics of Some Commonly Used Patterns

In a SerDes application the data pattern consists of user traffic and to a large extent patterns required for link management, clock ppm tolerance, idle channel fillers, word align, and many other primitives that are not scrambled. During training period at higher data rate application spectrally rich training patterns are available. But in mission mode SerDes sees both scrambled user traffic as well as non-scrambled nonuser data that are not suitable for continuous steady state operation of the SerDes. This section sheds some light on the spectral content of these patterns both in time domain and in frequency domain to get an intuitive feel for what kind of damaging effect they may impose on SerDes adaptation state.

Among many notorious patterns, CJTPAT is one of the most widely used pattern to stress SerDes CDR self-generated jitter using jitter tolerance metric as well as SerDes agility in maintaining its adaptation state. Why CJTPAT is a stress pattern can be viewed by

evaluating its spectral energy distribution, but a more direct feel can be obtained from its time domain view. In Figure 10 we present a cycle of CJTPAT passed through a 10m iPASS cable and we also present the FFT of the CJTPAT signal after it is filtered by a Gaussian pulse shaping filter operating at 64 oversampling rate. It is clear that there is a long stream of 1T Nyquist pattern that occupy a large fraction of the cycle which suffers the most attenuation at 6GHz while SerDes is operating at 12GT rate. This section of the pattern is bad both for CDR and adaptation point of view. During this period CDR will track the Nyquist pattern phase which is not favorable when more spectrally flat portion of the pattern segment appears. This manifests as a loss of CDR jitter tolerance margin. On the other hand, during this time if adaptation is allowed, the equalization parameters will start to optimize on Nyquist signal that is not optimal for user traffic that is mostly scrambled.

The second section of the ill-behaved pattern lies in the first segment of the pattern that is mostly dominated by 5T and 1T pattern. Again such bi-modal tone dominated pattern is also not favorable to adaptation, but CDR is less sensitive to it due to phase averaging effect.

The middle section of the pattern apparently looks like it is made out of mixed tone, but careful observation reveals that unlike in scrambled data this section has clusters of long and short run length signals that may not provide best adaptation. The CDR is lesser sensitive to this pattern clustering unless CDR is at a high gain state.

Up on viewing the spectral contents of the CJTPAT, above mentioned tone clustering is evident in the magnitude response shown in bottom pane of Figure 10. The magnitude response difference between the Nyquist (80dB) and average spectrum observed at 5T frequency location (41dB) is very large (39dB). We also observe tones dominance at Nyquist, half and quarter Nyquist, and other frequencies in between, making CJTPAT not a favorable pattern for SerDes operation, but a favorable pattern for stressing SerDes performance limit.

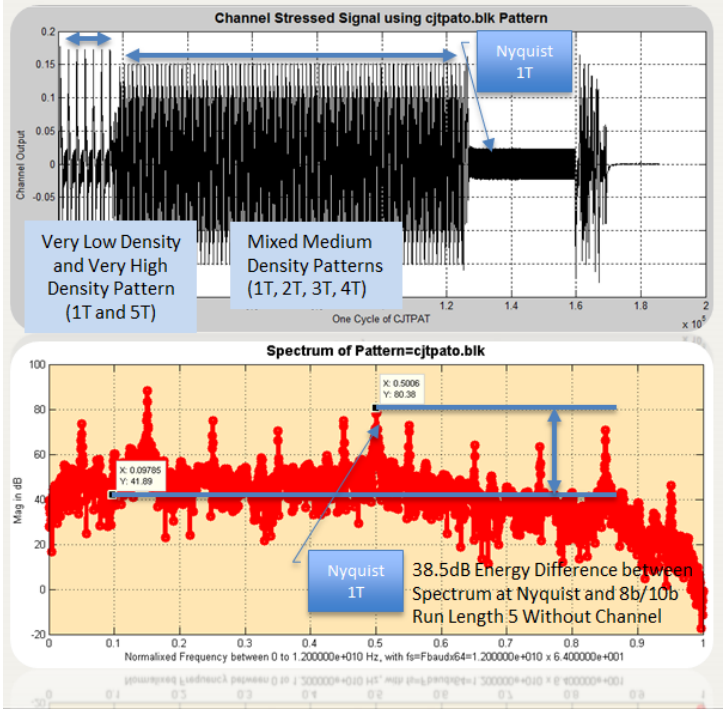
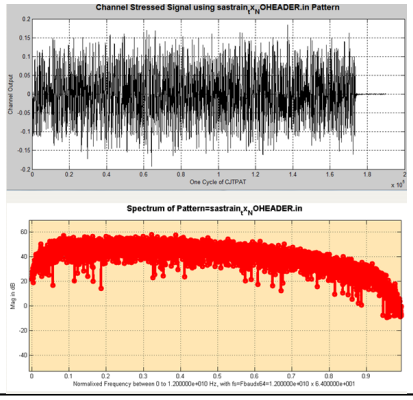
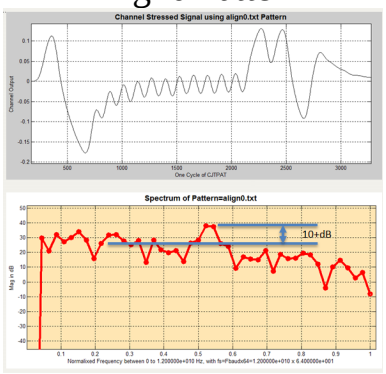
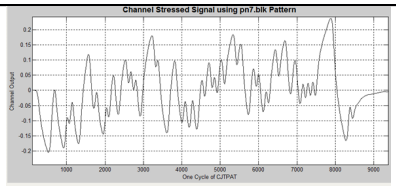


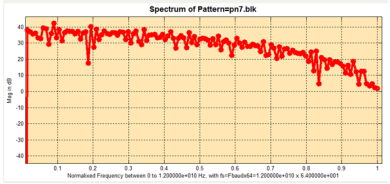
Figure 10: Time frequency domain view of CJTPA pattern

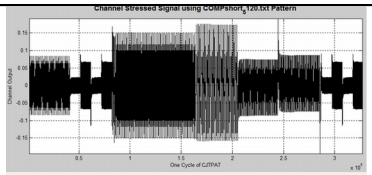
Some commonly used pattern in the SerDes validation and in our subsequent simulation is evaluated in time and frequency domain in table UU

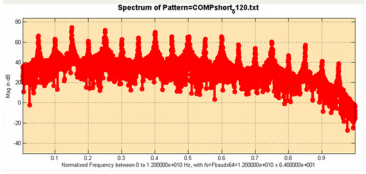
Table 4: Time and frequency domain view of some commonly used patterns

PATTERNS FAVORABLE TO SERDES OPERATION; PATTERNS WITH GOOD SPECTRAL CHARACTERISTICS	PATTERNS DETRIMENTAL TO SERDES OPERATION; PATTERNS WITH POOR SPECTRAL CHARACTERISTICS
SASTRAIN 	Align0 Pattern 
PN7	COMP_short Patten

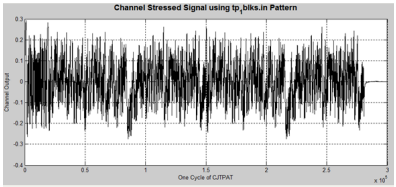


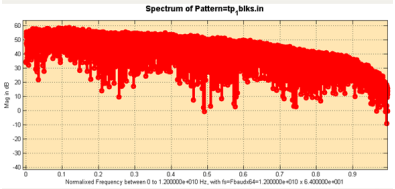




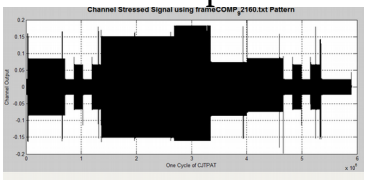


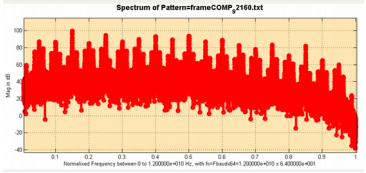
TP1 Pattern



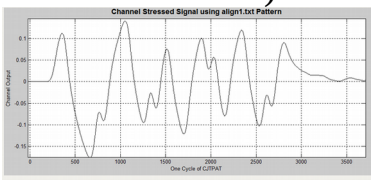


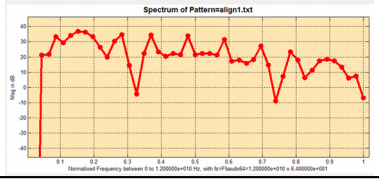
Frame Comp Pattern



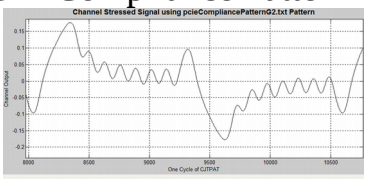


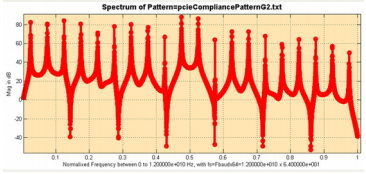
Align1 Pattern (less than Reasonable)





PCIE Compliance Pattern G2





A Time-Domain Frequency Discriminator for Detecting Pathological Segments in ill Patterns

A time domain equivalent frequency detection method and apparatus is presented in this section. The input sliced decisions are analyzed over a preset block of bits. For continuity of pattern analysis current block of data is overlapped with earlier block (or later block as one can envision). Over the overlapped block the distribution of 1T pattern is calculated by counting all 101 or 010 bit transitions. Similarly the distribution of 2T pattern is calculated by counting all occurrences of 0110 and 1001. Likewise the distribution of 4T pattern is calculated by counting all occurrences of 100001 and 011110. The distribution of 3T pattern is calculated by summing 1T and 2T pattern distribution. This method can be extended to any run length pattern.
The time domain pattern run length binning described above is equivalent to magnitude response in frequency domain. As for example, let's assume a N bit data block has all 1010 1T pattern. Using above mentioned binning technique a count of N-1 will be evaluated with a spectral line at N/2 with a scaling factor of 1. For 11001100 patterns the spectral line is at N/4 with a scaling factor of 2 and so on. This mimics the DFT function.

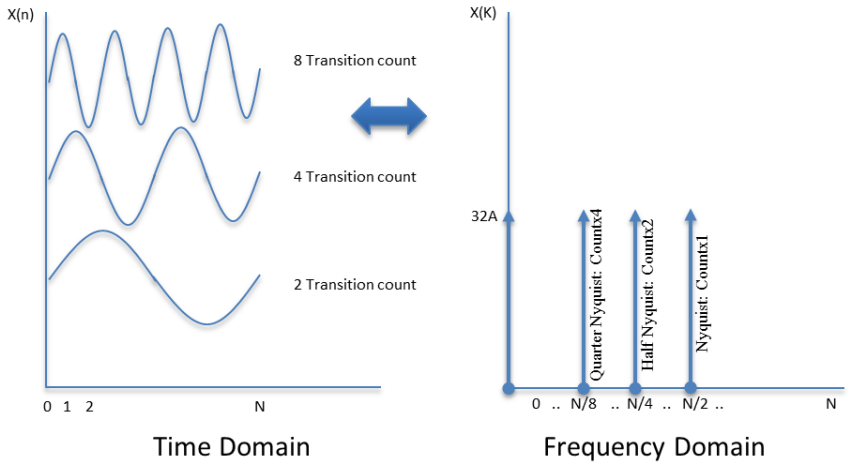


Figure 11: Classical DFT Time Frequency domain relationship

This example can be generalized for other above mentioned pattern run lengths. It is evident from above example that if the count value for 1T pattern exceeds a pre-defined threshold, this block of data will be dominated by a single tone and its characteristics will be non-random. Thus this block of data can be eliminated from going in to adaptation gradient calculation block [11] that expects data to be independent and identically distributed (IID). By following the spirit of this example for other tones, same argument can be established for other tones and tone combinations below Nyquist frequency. An apparatus [12] to detect the tones and tone combinations, evaluating each tone against a preset threshold, and asserting an adaptation freeze signal if the count exceeds the threshold over the evaluated block of pattern is presented in Figure 12. The tone threshold detection example uses CJTPAT as an example pathological pattern where adaptation should not be performed. When the Adaptation Freeze is asserted, the entire block of pattern is eliminated from gradient calculation.

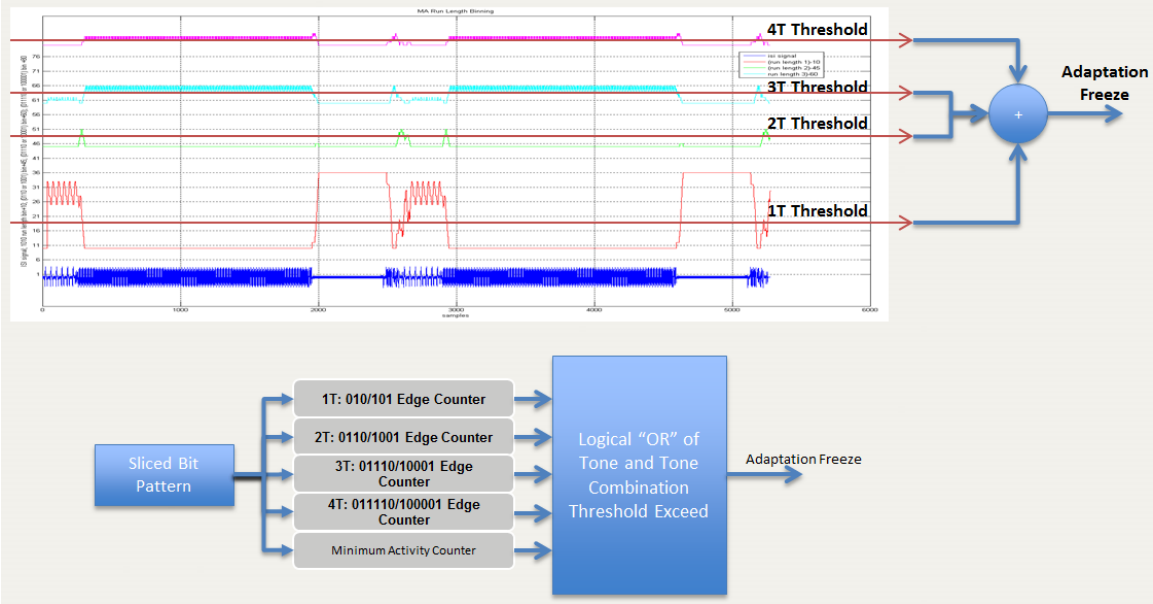


Figure 12: Pattern run length binning and adaptation inhibition on ill patterns

In case the adaptation freeze is asserted for an extended period of the, the CDR phase may drift to a suboptimal phase. If adaptation gradients are accumulated right after an extended adaptation freeze, the sampling point is not at desired phase and gathered adaptation error slicer information is not correct. As a result the adaptation freeze needs to be extended to allow for the CDR to reposition the sampling phases. This extension to above frequency discriminator is presented in Figure 13.

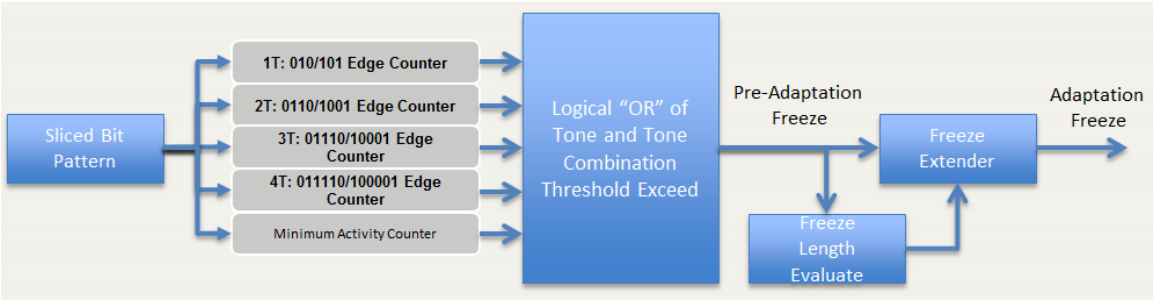


Figure 13: Adaptation freeze extender on extended freeze event

Pattern Discriminator Assisted Constrained DFE/LEQ/BCA Adaptation

The hardware configuration for the pattern Discriminator assisted receiver and transmitter adaption flow diagram is presented in Figure 14. The slicer decision is first analyzed by the pattern Discriminator and the input to the adaptation blocks are buffered up. First the pattern Discriminator evaluates the spectral contents of the input data block. If received

sliced data is acceptable for adaptation the adaptation freeze pin is de-asserted and buffered data is used for DFE, linear equalizer, and back channel coefficient update. On the other hand if the input sliced data set is not suitable for adaptation the adaptation freeze pin is asserted and the adaptation block discards the buffered data set.

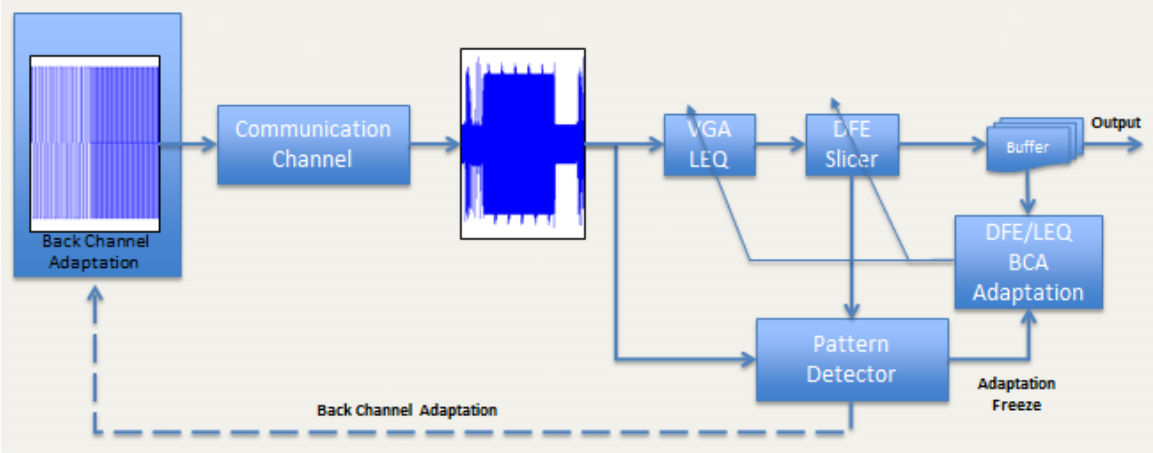


Figure 14: Pattern Discriminator assisted constrained DFE/LEQ/BCA adaptation

The performance of the pattern Discriminator is evaluated, in simulation and in hardware, by cascading three types of pattern sequences for initial training and subsequent adaption mistuning, and EYE margining. The pattern set used in this experiment is presented in Figure 15.

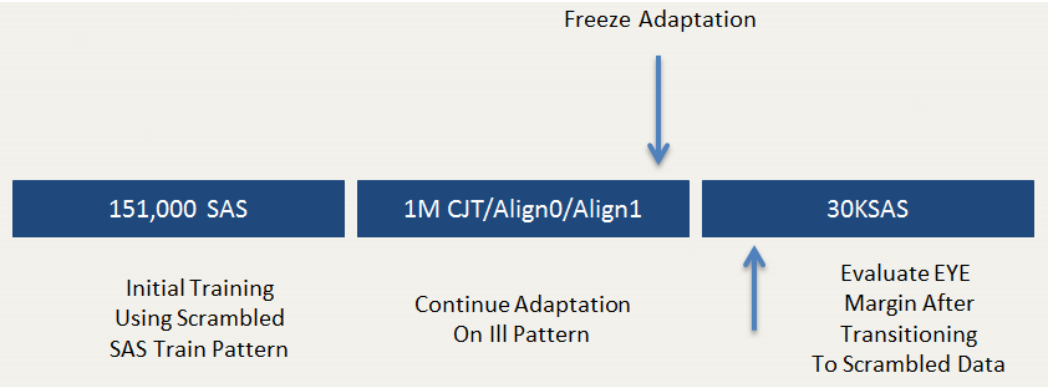


Figure 15: Pattern sequence for evaluation pattern Discriminator effectiveness

The initial training of the transceiver is performed using scrambled data pattern (SAS train pattern). Next the receiver is treated with selected pathological pattern. In one case the receiver is allowed to adapt by turning off the pattern Discriminator and in another case the receiver is allowed to perform pattern Discriminator constrained adaptation. Next, the adaptation is frozen at the end of the pathological pattern, and receiver input

pattern is switched to scrambled pattern. On the scrambled pattern the receiver noise and jitter margin is measured.

In the experiment below during initial 150K UI the receiver adapted to healthy EYE margin. During the next 1M UI the input pattern is switched to CJTPAT and the pattern Discriminator is turned off. The receiver continued to adapt. During this time the linear equalizer adapted to a much smaller boost and the DFE taps builds up that is not suitable for scrambled data EYE margin. At the end of the 1M UI of CJTPAT the receiver adaptation is frozen. Next the pattern is switched to scrambled pattern. After the receiver mistuned its adaptation parameters, the receiver was not at optimal settings for the scrambled pattern. The resulting DFE EYE did not have operating margin as shown in Figure 16.

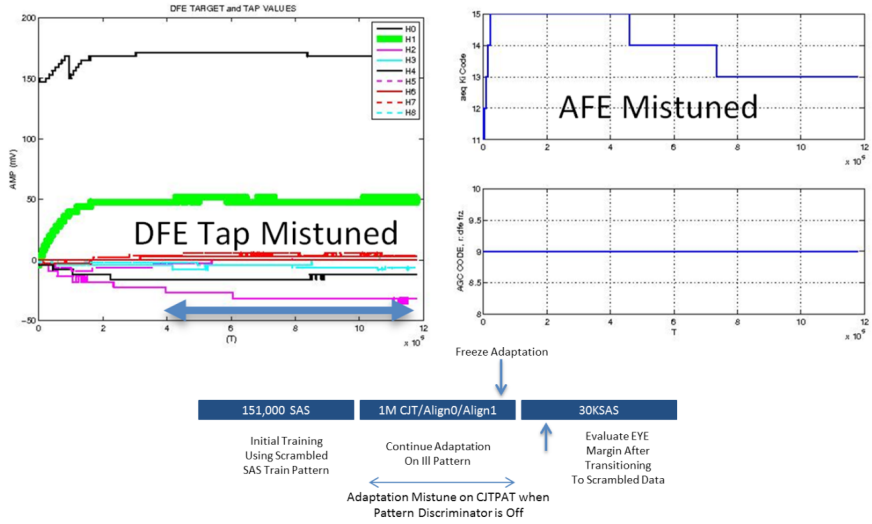


Figure 16: In absence of pattern Discriminator assisted adaptation the receiver mistuned over CJTPAT

Next we repeat the same experiment, but in this case we turn on the pattern Discriminator. Pattern Discriminator detected the presence of ill patterns in CJTPAT and asserted adaptation freeze over the entire 1M UI CJTPAT. As a result the DFE tap, LEQ, and VGA remained at their initial adapted settings. When the scrambled pattern came in, the adaptation settings were suitable for its support and the EYE margin offered healthy operating values as shown in Figure 17.

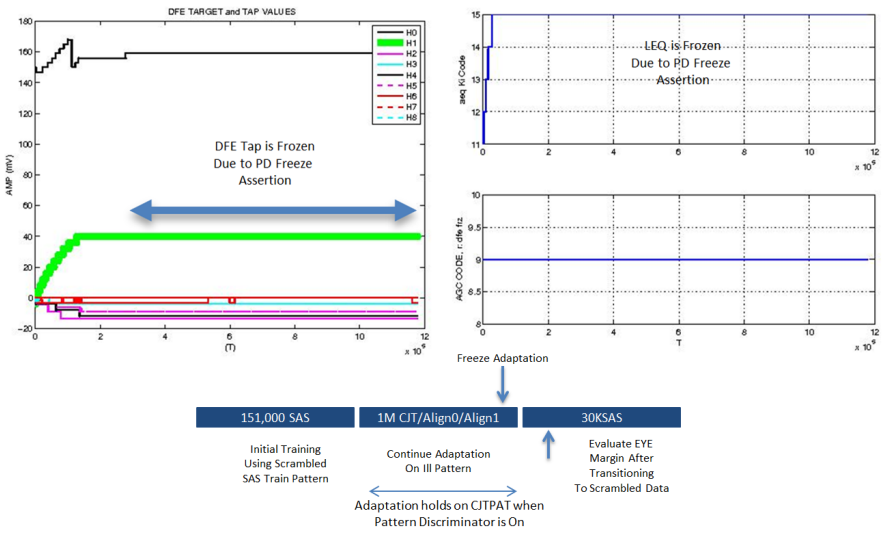


Figure 17: Pattern Discriminator constrained receiver adaptation froze all equalization on CJTPAT

Evaluate Steady State Adaptation Performance Using Pattern Discriminator

To demonstrate the effectiveness of the pattern discriminator constrained steady state adaptation, a 12G SAS simulation setup is used. The pattern sequence shown in Figure DC is used in following simulation combination. The EYE margins obtained in various operating conditions are compared with EYE margin obtained when the transceiver is adapted with spectrally rich scrambled pattern.

> Test Case 1: Turn off pattern discriminator. Perform initial adaptation on 151K UI SAS scrambled data pattern, then continue to adapt on 1M UI pathological pattern and freeze adaptation then switch to 30K UI scrambled data to measure EYE margin. The objective is to see the effect of any adaptation degradation over the pathological patterns.
>
> Test Case 2, 3, 4, 5, 6: Same as test case 1, but turn on pattern discriminator constrained adaptation using 5 different pattern discriminator threshold settings for the tones. The objective of this test is to evaluate quantitative EYE margin recovery using the pattern discriminator constrained adaptation.

The goal of the pattern Discriminator is to discard patterns that are unfavorable for reliable adaptation and allow adaptation on favorable patterns that are not tone dominated. As a result, adaptation can remain frozen at its initial training adapted values on the second pathological pattern segment defined above. The tone threshold of the pattern Discriminator can be adjusted to be too conservative or too relaxed with unfavorable adaptation results in either case. Optimal threshold is determined empirically. For each simulation run we report adapted values of {AGC, LEQ, DFE Tap1, and DFE Tap2} followed by Vertical EYE margin in mVp and Horizontal EYE Margin in UIpp.

In the first set of data adaptation was performed with scrambled data. For long channel the peak vertical EYE opening is 89mVp and the peak-peak horizontal EYE opening, defined as 2*min(left H opening, UIL, right H opening, UIR), is 0.63UIpp. In the second set of data, adaptation was done with CJTPA pathological pattern after initial adaptation with scrambled data, without turning on the pattern discriminator, and EYE margining was performed on scrambled data after adaptation was frozen on pathological pattern. The peak vertical EYE opening reduced to 9.7mVp and the peak-peak horizontal opening reduced to 0.25UIpp. In subsequent set of data pattern discriminator was turned on from the beginning. In these set of data the pattern discriminator tone thresholds was adjusted to be conservative and pessimistic and values in between them. When threshold for tome detector was too low the adaptation was blocked most often and transceiver could not be optimized. When the threshold was too high, adaptation was never blocked even on the pathological segment. At empirically optimized moderate threshold setting adaptation was optimized but not as good as in free adaptation on scrambled data, but was good enough and adaptation never diverged as in free adaptation case over pathological pattern segment. In Table 5 a summary of the EYE margin is presented for adaptation on scrambled data without pattern discriminator, adaptation on pathological pattern after initial adaptation over scrambled pattern without using pattern discriminator, and finally adaptation on scrambled followed by pathological pattern using pattern discriminator with empirically optimized thresholds. It is evident from these simulation results that pattern discriminator constrained adaptation halts adaptation from diverging on pathological pattern providing good margin, but is not as good as with scrambled patterns.

Table 5: Pattern discriminator performance on long channel

PATTERN DISCRIMINATOR EVALUATION ON LONG CHANNEL USING CJTPAT AS THE PATHOLOGICAL PATTERN.

ADAPTATION WITH SCRAMBLED PATTERN		ADAPTATION CONTINUE ON CJTPAT WITH PD OFF		ADAPTATION CONTINUE ON CJTPAT WITH PD ON	
VM	HM	VM	HM	VM	HM
89	0.63	9.7	0.25	66	0.50

Pattern discriminator evaluation on long channel using ALIGN1 as the pathological pattern.

Adaptation with scrambled pattern		Adaptation continue on CJTPAT with PD off		Adaptation continue on CJTPAT with PD on	
VM	HM	VM	HM	VM	HM
89	0.63	42	0.32	71	0.53

Pattern discriminator evaluation on long channel using frameComp as the pathological pattern.

Adaptation with scrambled pattern		Adaptation continue on CJTPAT with PD off		Adaptation continue on CJTPAT with PD on	
VM	HM	VM	HM	VM	HM

89	0.63	35	0.41	72	0.56

Pattern discriminator evaluation on short channel using CJTPAT as the pathological pattern.

Adaptation with scrambled pattern		Adaptation continue on CJTPAT with PD off		Adaptation continue on CJTPAT with PD on	
VM	HM	VM	HM	VM	HM
102	0.56	73	0.44	105	0.56

Pattern discriminator evaluation on short channel using COMP_Framed_RD as the pathological pattern.

Adaptation with scrambled pattern		Adaptation continue on CJTPAT with PD off		Adaptation continue on CJTPAT with PD on	
VM	HM	VM	HM	VM	HM
102	0.56	78	0.41	103	0.56

Pattern discriminator evaluation on short channel using frameCOMP as the pathological pattern.

Adaptation with scrambled pattern		Adaptation continue on CJTPAT with PD off		Adaptation continue on CJTPAT with PD on	
VM	HM	VM	HM	VM	HM
102	0.56	69	0.41	101	0.56

Illustrate the effectiveness of the pattern discriminator for steady state adaptation for PCIe Gen4 and SAS4

PCIe Gen4 with 16GT/s continues with PCIe Gen3 like 128b/130b encoded frames with data being scrambled using a PN23 scrambler. For clock ppm tolerance periodically Skip Order Set (SOS) pattern is transmitted for FIFO relief [9] that can consume close to 3% of the bus bandwidth [15]. AT the moment PCIe Gen4 is leaning towards 28dB channel loss at 8GHz based on studies performed by IBM and Intel. In storage front SAS Gen4 with 20-24GT/s adopted PCIe like 128b/130b encoded frames with data being scrambled using a PN23 scrambler with channel loss up to 30dB at the pin [10].
We evaluate the PCIe Gen4 and SAS4 performance with and without pattern discriminator using a 28dB channel @8GHz and 30dB channel @12GHz respectively. Results show that no significant difference with and without pattern discriminator.

Table 6 PCIe Gen4 and SAS4 evaluation with PD using 28dB and 30dB channel

TX SETTING	NO PATTERN DISCRIMINATOR VOLTAGE MARGIN MVP	JITTER MARGIN UIPP	PATTERN DISCRIMINATOR VOLTAGE MARGIN MVP	JITTER MARGIN UIPP
SAS4 TX no Emphasis	70mVp	0.406UIpp	66mVp	0.406UIpp

SAS4 TX with 2.5dB Pre-Emphasis	81mVp	0.5UIpp	87mVp	0.5UIpp
PCIE4 TX no Emphasis	121mVp	0.56UIpp	116mVp	0.68UIpp
PCIE4 TX with 2.5dB Pre-Emphasis	112mVp	0.53UIpp	116mVp	0.59UIpp

The reason is that the pathological SOS pattern that has 1010 sequence is a small percentage of the rest of the PN23 scrambled pattern to cause detrimental effect on the adapted equalization parameters. If a continuous steady state adaptation is performed without a pattern detector a robust operating margin can be maintained, provided supporting equalization range is available to accommodate the channel loss, at the expense of increased power dissipation. If periodic steady state operation is desired, to minimize the operating power, a pattern discriminator is necessary to safeguard against adaption compromise over SOS pattern.

Conclusion

Temperature, humidity, and slow voltage variation over time is inevitable that renders initial adaptation values not optimal at prolonged steady state operation. Periodic adjustment to receiver equalization parameters is necessary for maintaining good operating noise and jitter margin. But good scrambled data pattern is not guaranteed is mission mode of operation carrying live traffic. This paper offers a method and apparatus to detect presence of pathological pattern that are not favorable for adaptation and allows a constrained transceiver adaptation only when presence of spectrally rich pattern is detected.

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